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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J41 MLB SCHEMATIC 6.6.0

DVT

4/09/13

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9795	1	SCHEM,MLB,J41	SCH	CRITICAL	
820-3435	1	PCBF,MLB,J41	PCB	CRITICAL	

DRAWING

TITLE-MLB

ABREV-DRAWING

DATE: 20130910 10:46 AM

PRODUCT SAFETY REQUIREMENTS:

PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.

PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE

<PART_DESCRIPTION>

Apple Inc.

<SCH_NUM>

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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE , COMMON , MLB_MISC , MLB_DEBUG : ENG , MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO , TBTHV:P15V , EDP , CAM_XTAL:NO , CAM_WAKE:NO , APCLKRQ:ISOL , TPAD_INTWAKE:SHARED , USB_PWR:S3 , SD_ON_MLB , VCORE_FETS
MLB_DEVEL:ENG	ALTERNATE , BKLT:ENG , XDP_CONN , DDRVREF_DAC , S0PGOOD_ISL , DBGLED , ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	DEVEL_BOM , XDP , LPCPLUS
MLB_DEBUG:PVT	DEVEL_BOM , BKLT:PROD , XDP , LPCPLUS , ISNS:PROD
MLB_DEBUG:PROD	BKLT:PROD , LPCPLUS , XDP , ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_1SNS:YES,CPUOV_1SNS:YES,DRAM_1SNS:YES,P1V05_1SNS:YES,AIRSPORT_1SNS:YES,SSD_1SNS:YES,LCDBELT_1SNS:YES,P1V35_1SNS:YES,IY350_1SNS:YES,OTHER_HS_1SNS:YES,CAN_1SNS:YES,CPUDDR_1SNS:YES,PANEL_1SNS:YES
ISNS:PROD	CPU_HS_1SNS:YES,CPUOV_1SNS:YES,DRAM_1SNS:YES,P1V05_1SNS:NO,AIRSPORT_1SNS:NO,SSD_1SNS:YES,LCDBELT_1SNS:NO,P1V35_1SNS:NO,IY350_1SNS:NO,OTHER_HS_1SNS:NO,CAN_1SNS:NO,CPUDDR_1SNS:NO,PANEL_1SNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:MICRON_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U2890	CRITICAL	TBTR0M:BLANK
341S3802	1	IC,EEPROM,C/R (V23.4) EVT,741/741	U2890	CRITICAL	TBTR0M:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50MDIPS MCU,9X9,157BGA	U5000	CRITICAL	SMC:BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S3809	1	IC,EPI ROM (V0071) DVT,741/743	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW, SR16M, PRQ, CO, 1.3, 15W, 2+3, 1.0, 3M, BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW, SR16L, PRQ, CO, 1.4, 15W, 2+3, 1.1, 3M, BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW, SR16H, PRQ, CO, 1.7, 15W, 2+3, 1.1, 4M, BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC, TBT, CR-4C, B1, PRQ, C10, 288, 12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC, BCM15700A2, S2 PCIe CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY, SUBASSY, PCBA, HALL EFFECT, K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 HLM DPMX ADHESIVE 29993-BC 0.4G	GLUE	CRITICAL	
825-7670	1	LABEL, TEXT, MLB, K21/K78	LABEL		
376S0964	2	MOSFET, N-CH, 25V, 30A, 9.6M, 8P 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET, N-CH, 25V, 30A, 6.1M, 8P 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET, N-CH, 30V, 15.3A, 12M, 8P 3.3X3.3 DFN	Q7310, Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET, N-CH, 30V, 22A, 6.0M, 8P 3.3X3.3 DFN	Q7311, Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=HYNIX_4Gb
333S0681	4	IC, SDRAM, 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=HYNIX_8Gb
333S0676	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=SAMSUNG_4Gb
333S0680	4	IC, SDRAM, 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=SAMSUNG_8Gb
333S0678	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=ELPIDA_4Gb
333S0666	4	IC, SDRAM, 16Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=ELPIDA_8Gb
333S0679	4	IC, SDRAM, 8Gb, LPDDR3-1600, 178P FBGA	U2300, U2400, U2500, U2600	CRITICAL	DRAM_TYPE=MICRON_4Gb

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NEK alt for Diodes dual
376S1089	376S1128		ALL	NEK alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cytotec
372S0186	372S0185		ALL	NEK alt to Diodes
197S0479	197S0478		ALL	200uW Epcos alt to NEK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cytotec alt to NEC
197S0480	197S0343		ALL	NEK crystal alt to TSC
197S0481	197S0343		ALL	Epcos crystal alt to TSC
107S0254	107S0241		ALL	Cytotec sense R alt to TFF
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NEK alt to TSC
197S0545	197S0544		ALL	Epcos alt to TSC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Remesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cytotec alt to TFF
107S0250	107S0248		ALL	Cytotec alt to TFF

CPU DRAM CFG Chart

	VENDOR	CFG 1	CFG 0
	HYNIX	0	0
	SAMSUNG	1	0
	MICRON	0	1
	ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4118	PCBA,MLB,BEST,HY 4GB,J41:	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4274	PCBA,MLB,BEST,HY 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4275	PCBA,MLB,BEST,EL 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4276	PCBA,MLB,BEST,EL 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4702	PCBA,MLB,BEST,MI 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
639-4434	PCBA,MLB,BETTER,HY 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4435	PCBA,MLB,BETTER,HY 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4436	PCBA,MLB,BETTER,EL 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4437	PCBA,MLB,BETTER,EL 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4703	PCBA,MLB,BETTER,MI 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
685-0024	CMN PTS,PCBA,MLB,J41	MLB_COMMON,J41_MLB
985-0017	J41 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0062	VCORE FET,REN,J41	VCORE_FET:REN
685-0063	VCORE FET,VSHY,J41	VCORE_FET:VSHY

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG, SMC:PROG, TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3757	1	IC,SMC-A3 SCPL,EXT,V22,12A18,PROTO 1,J41	U5000	CRITICAL	SMC:PROG


Alternate Parts

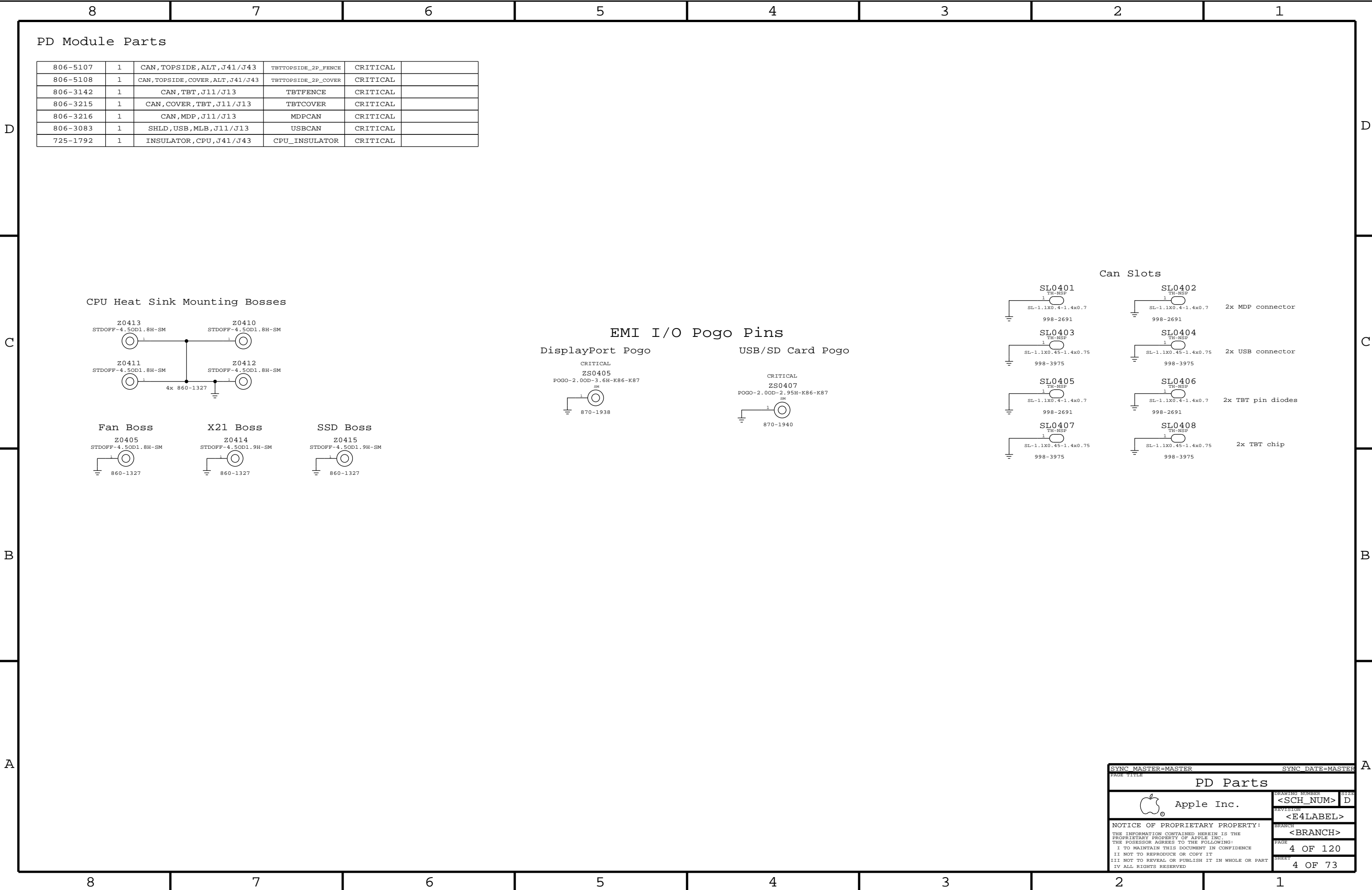
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0062	685-0063		ALL	Renaseas alt to Vishay

333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix
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Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0017	1	J41 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0024	1	CMN PTS,PCBA,MLB,J41	CMNPTS	CRITICAL	MLB_CMNPTS
685-0063	1	VCORE FET,VSHY,J41	VCOREFETS	CRITICAL	VCORE_FETS

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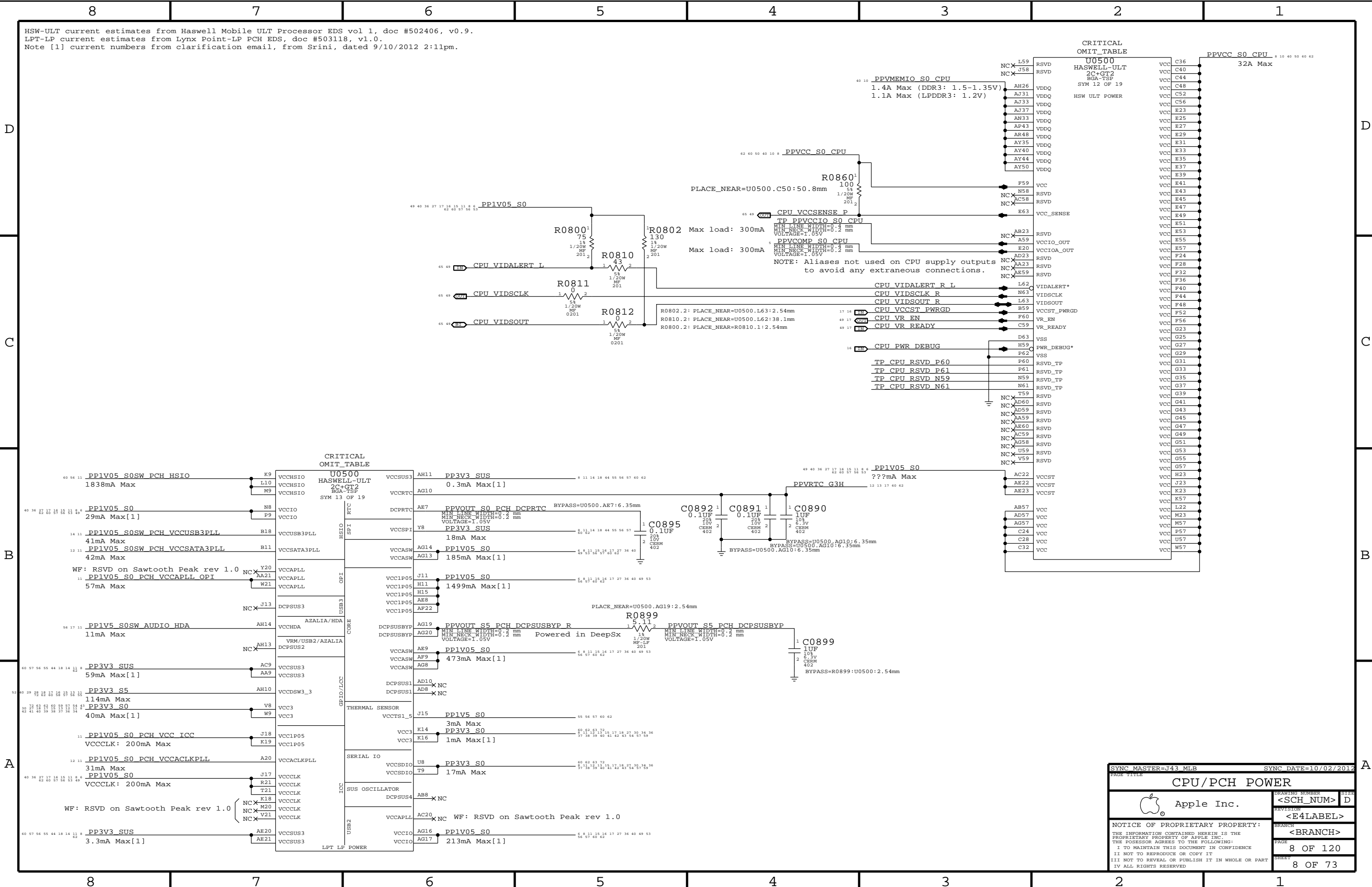


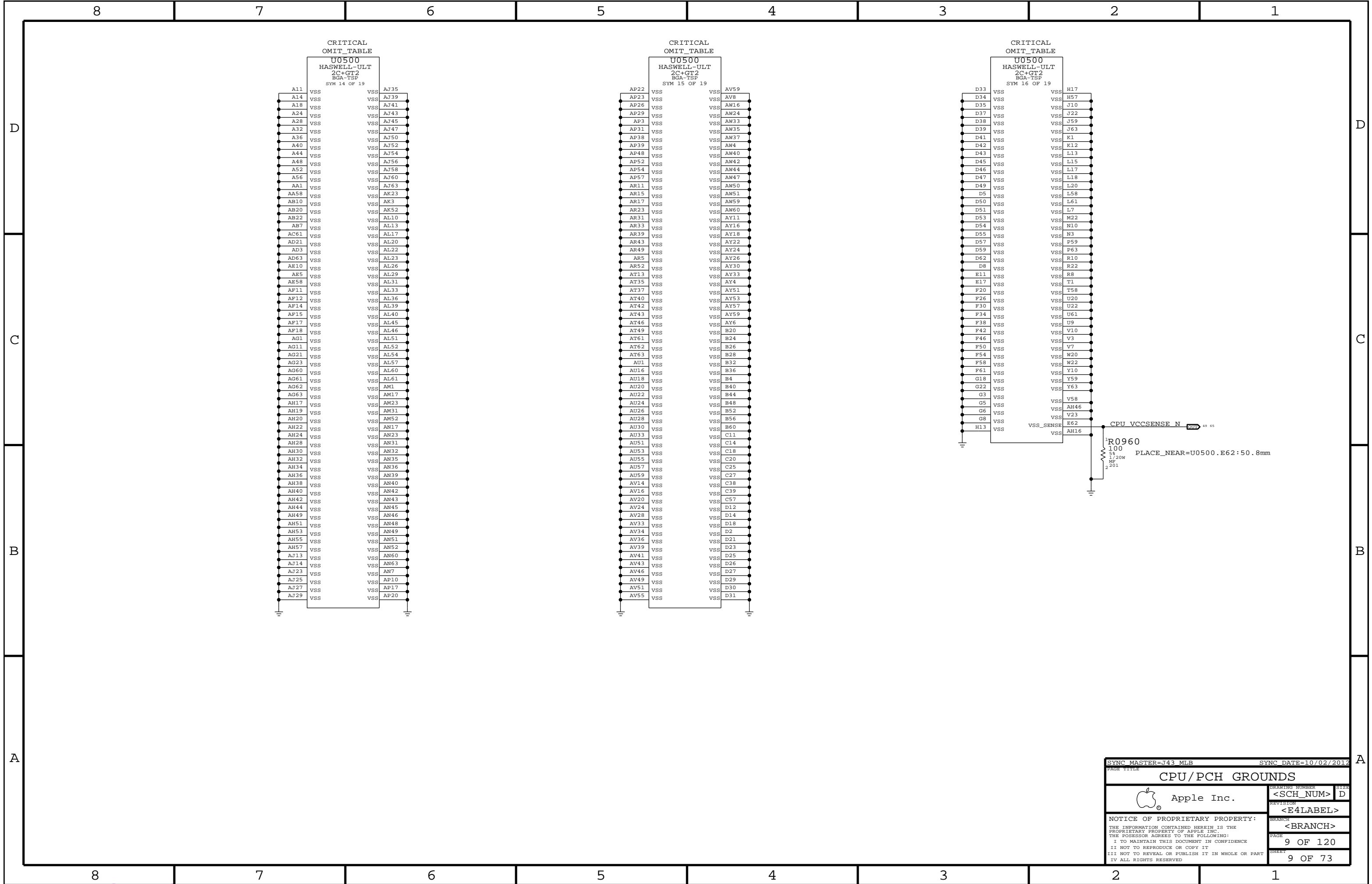


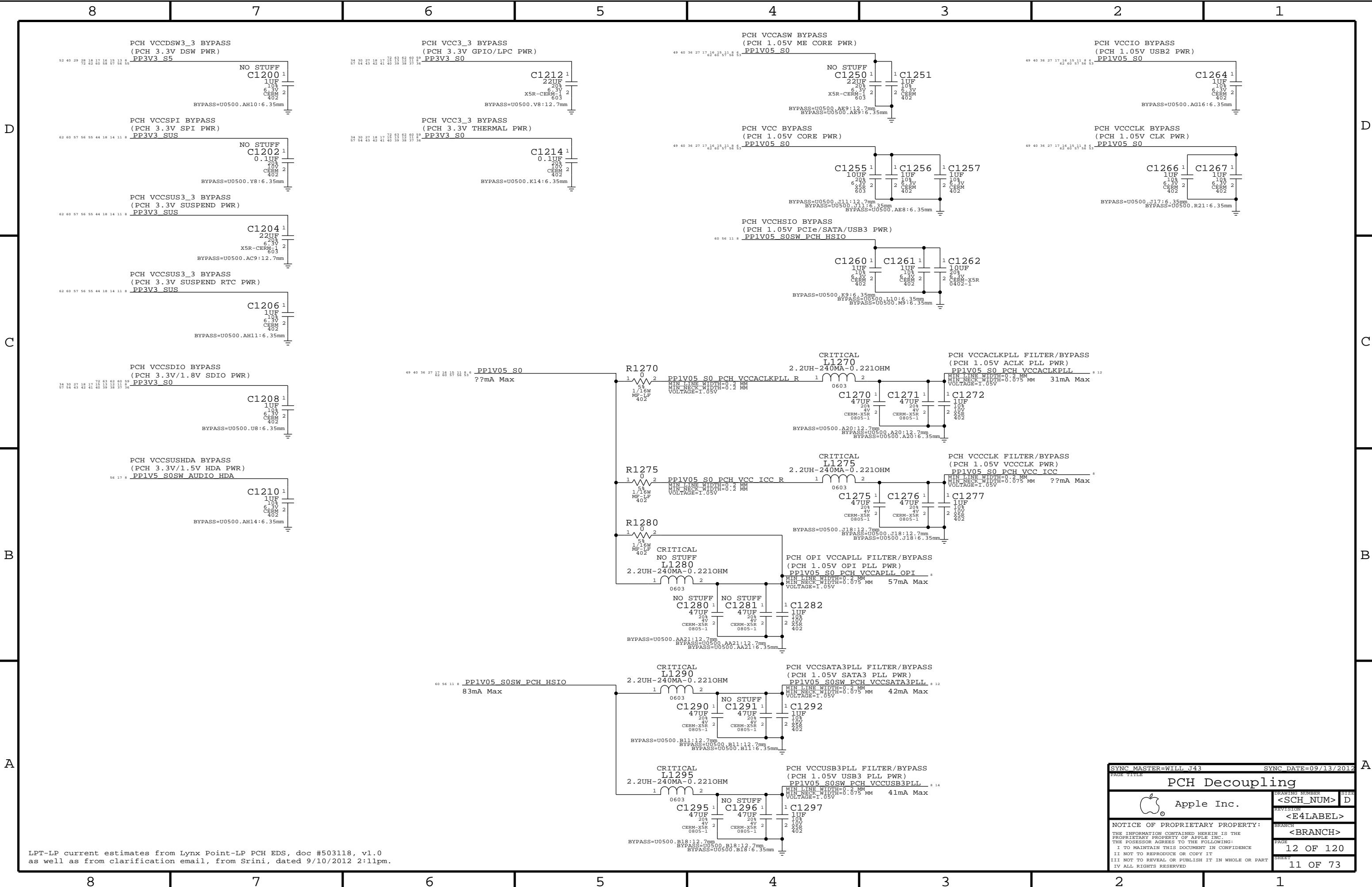
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LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srinii, dated 9/10/2012 2:11pm.

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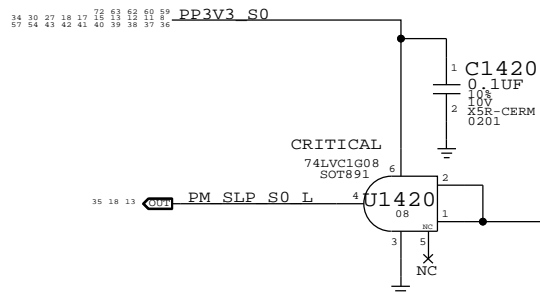
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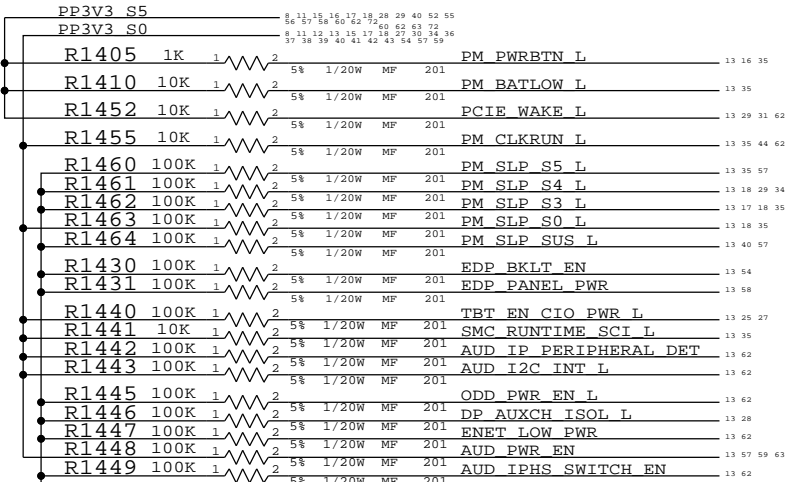
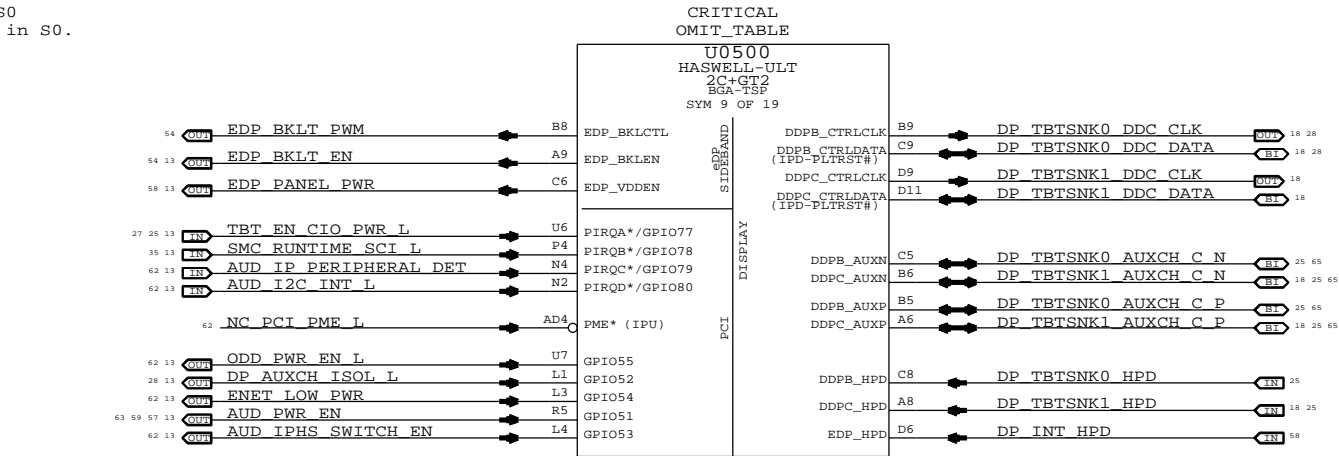
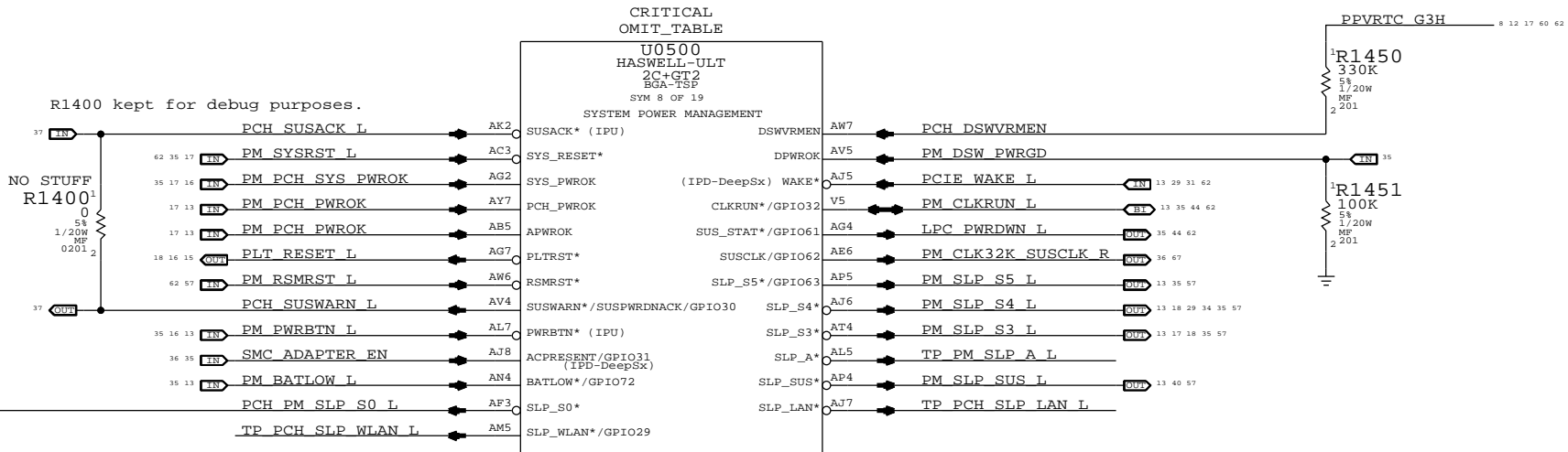
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SLP_S0# Isolation



SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.



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PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 11 OF 19

CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 7 OF 19

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

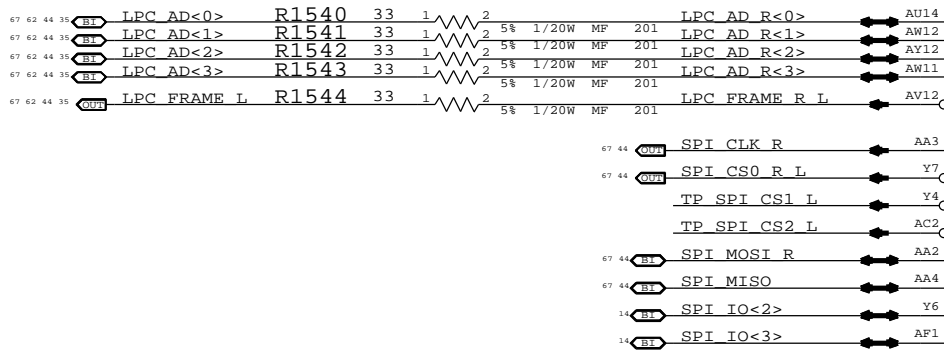
Reserved: SD (HS)

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

SML1ALERT# pull-up not provided on this page, may be wire-0Red into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

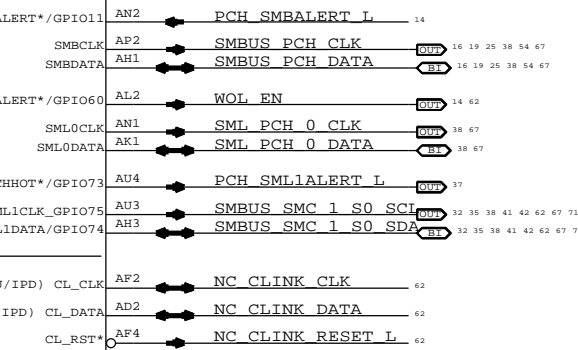


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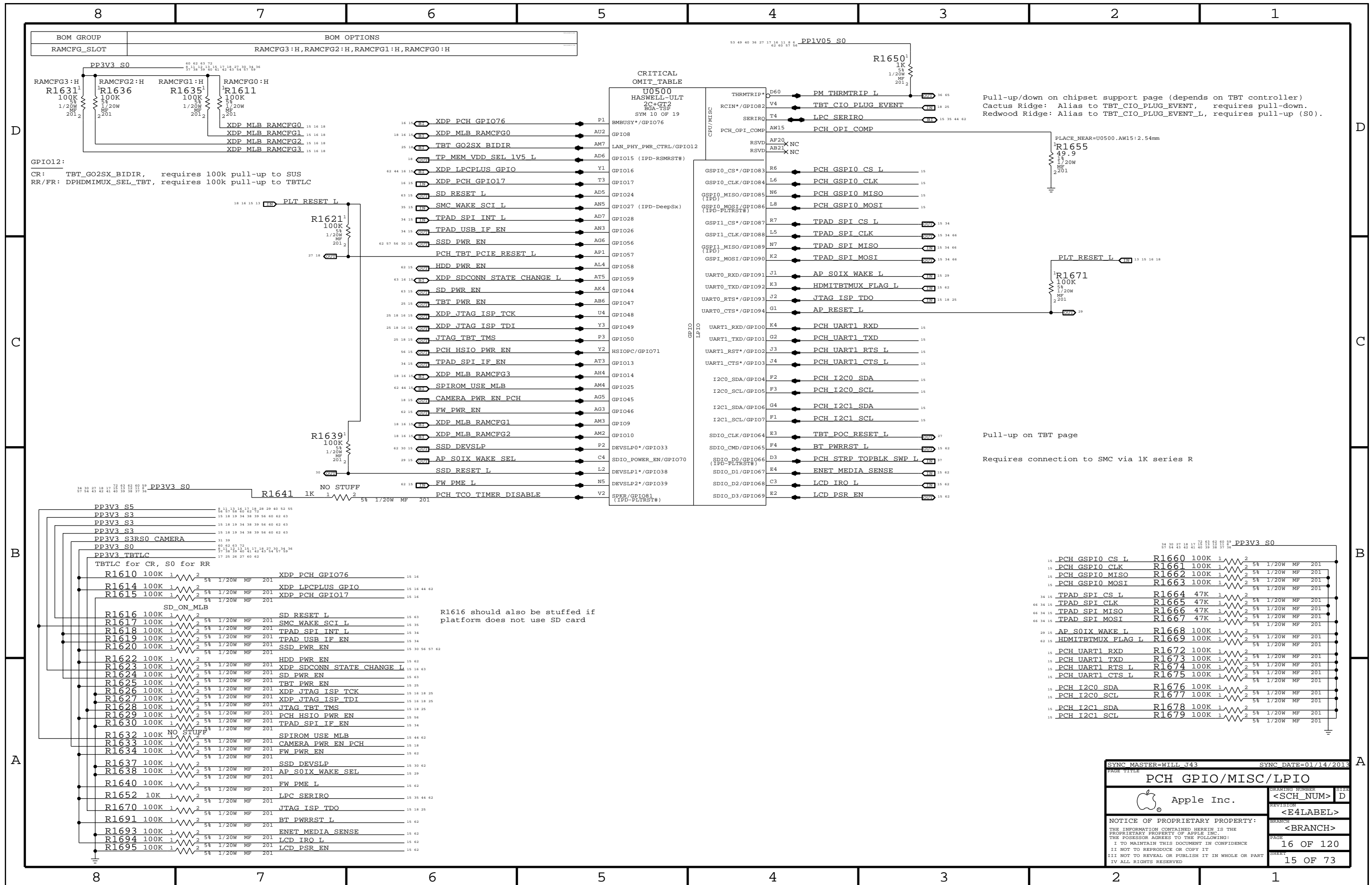
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 7 OF 19

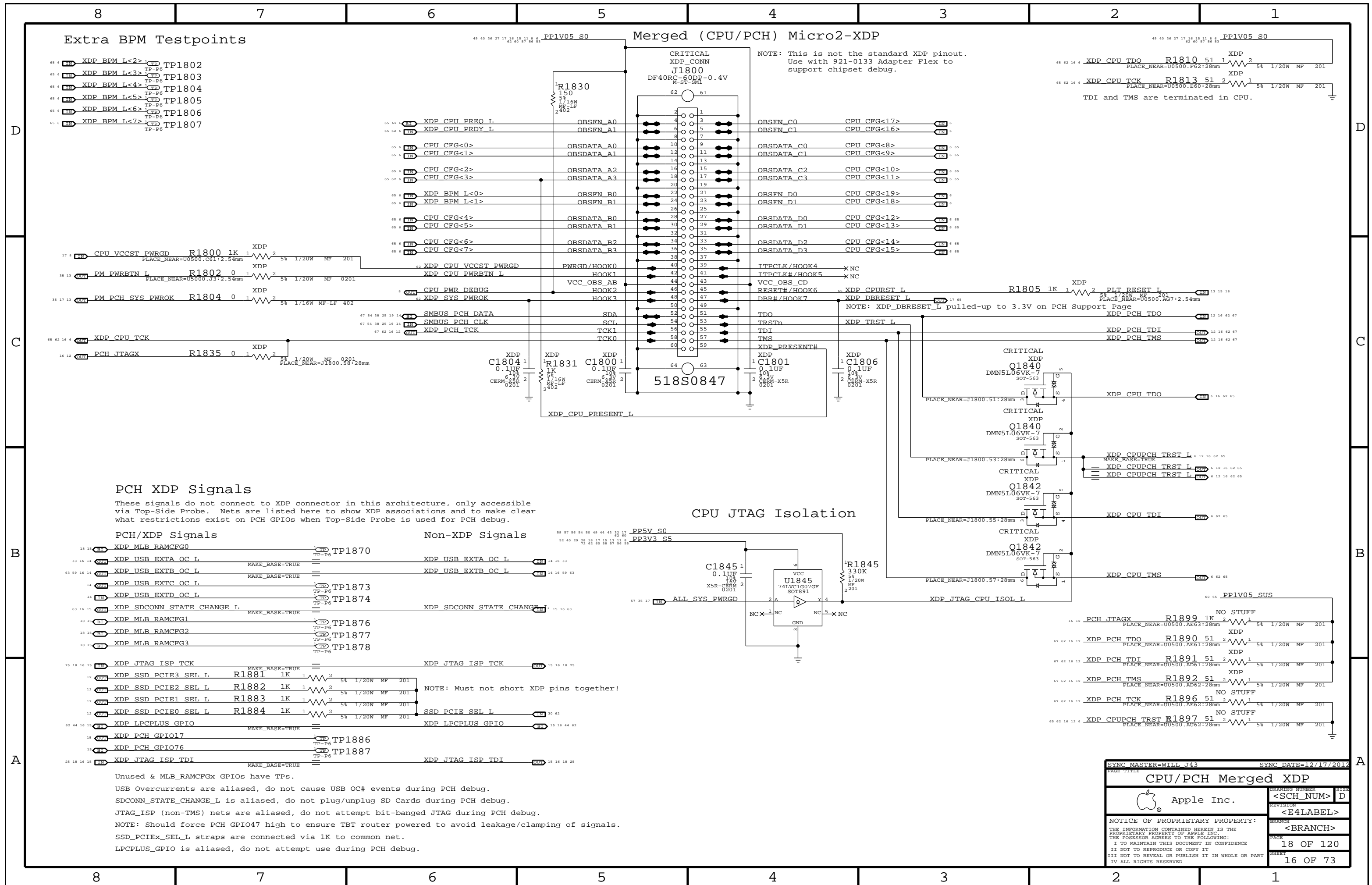
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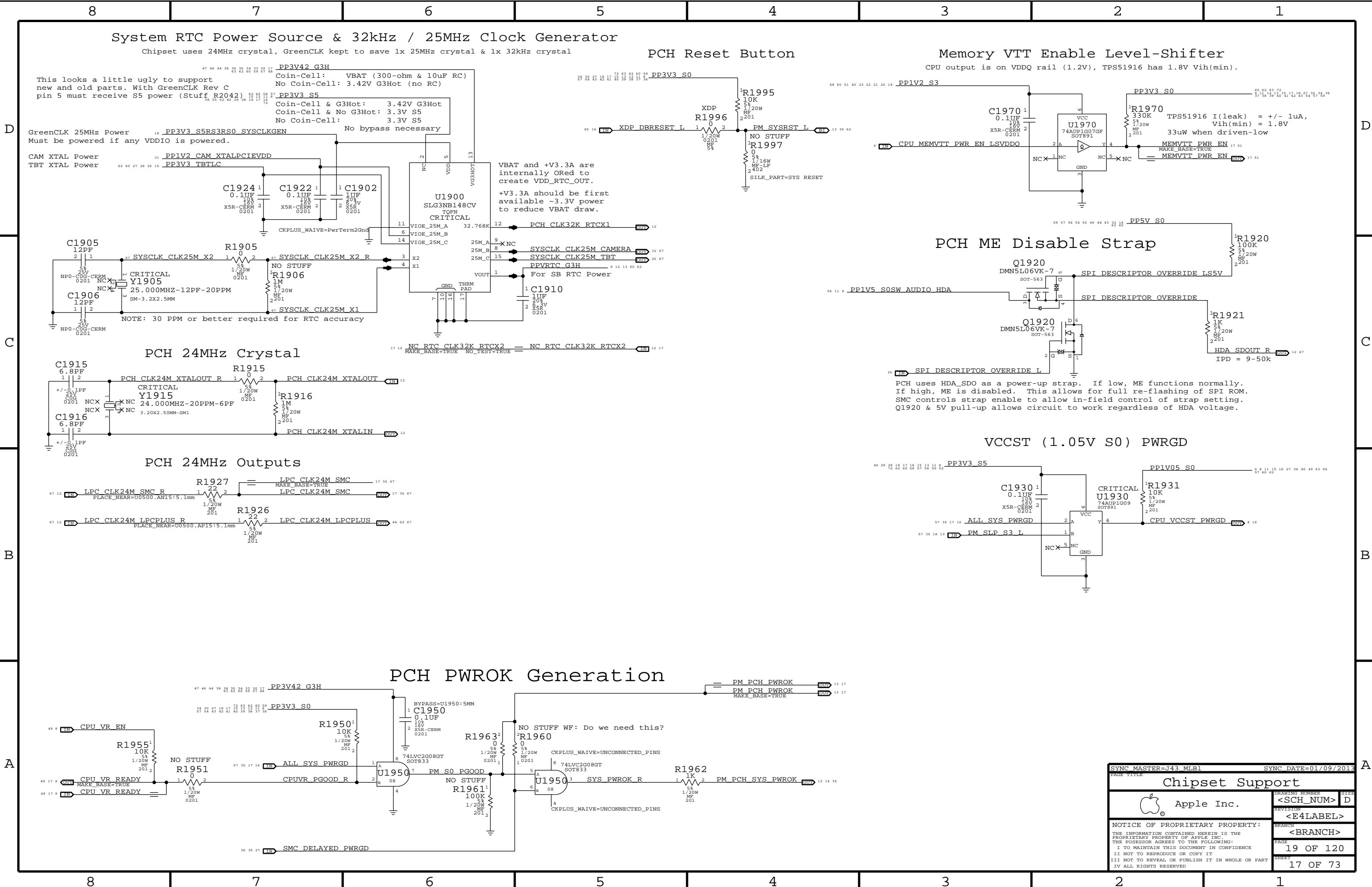
U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 7 OF 19




SYNC MASTER=WILL J43		SYNC DATE=09/13/2012	
PAGE TITLE			
PCH PCIe/USB/LPC/SPI/SMBus			
Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=J43 MLB1		SYNC DATE=01/09/2013	
PAGE TITLE			
Chipset Support			
 Apple Inc.		DRAWING NUMBER	SIZE
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IV ALL RIGHTS RESERVED			

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

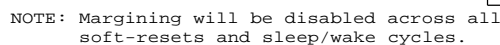
BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

FETs for CPU isolation during DAC margining

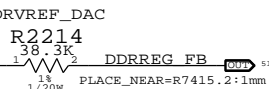
NOTE: CPU has single output for VREFOA. Split into two signals for independent DAC margining support. When DAC margining VREFOA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

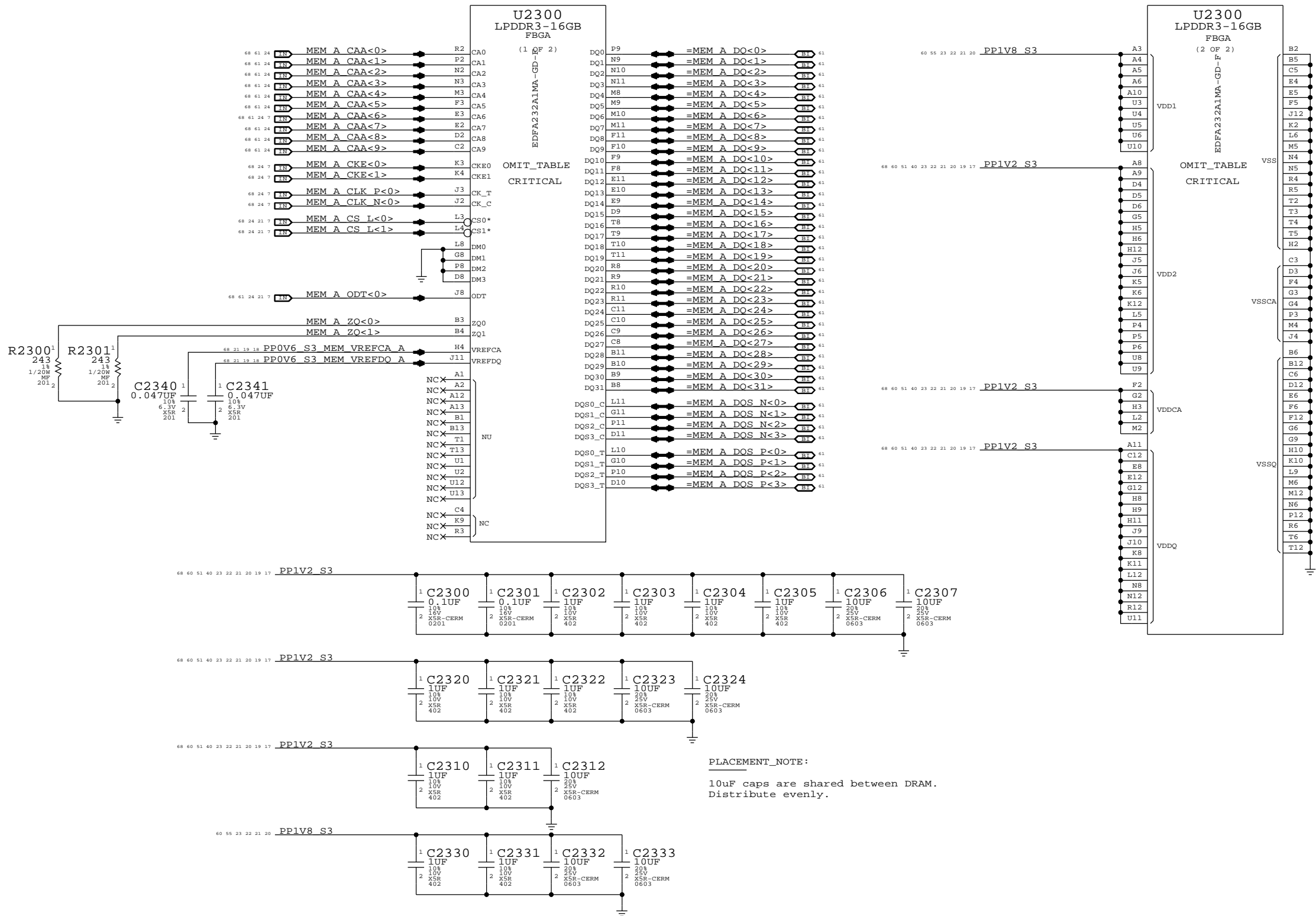



NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

Always used, regardless
of margining option.

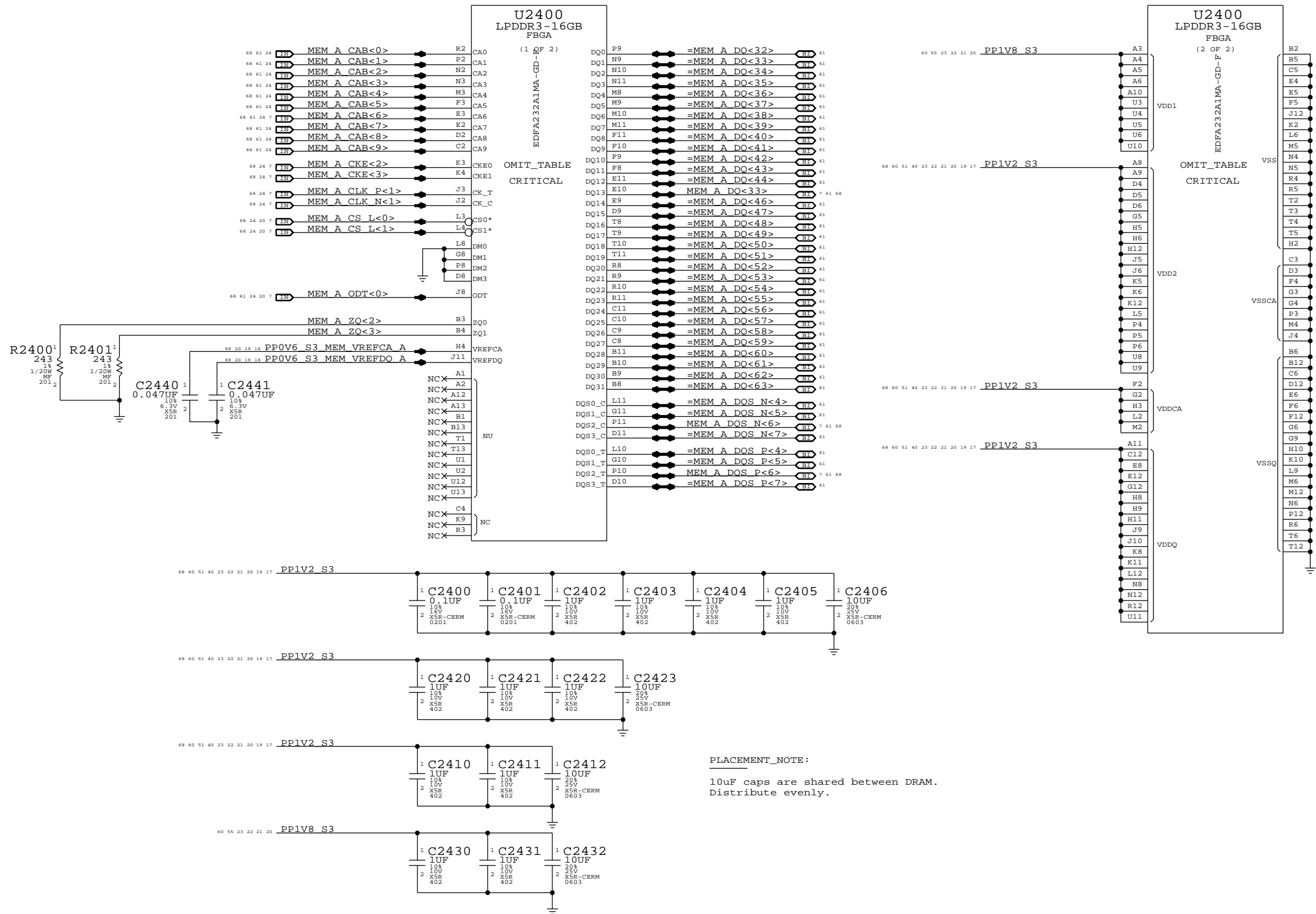



LPDDR3 CHANNEL A (0-31)



SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
LPDDR3 DRAM Channel A		A (0-31)	
	DRAWING NUMBER		SIZE
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PAGE		23 OF 120	
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LPDDR3 CHANNEL A (32-63)



SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
LPDDR3 DRAM Channel A		(32-63)	
	DRAWING NUMBER		SIZE
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		BRANCH	
		<BRANCH>	
PAGE		24 OF 120	
SHEET		21 OF 73	

D



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B

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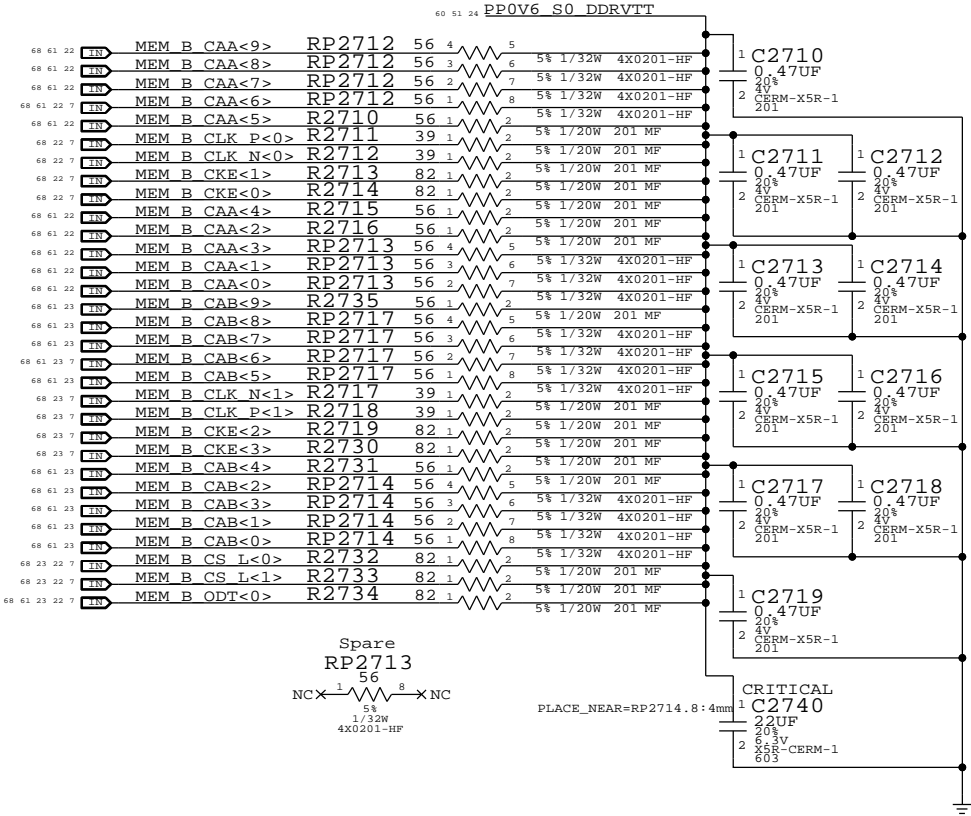
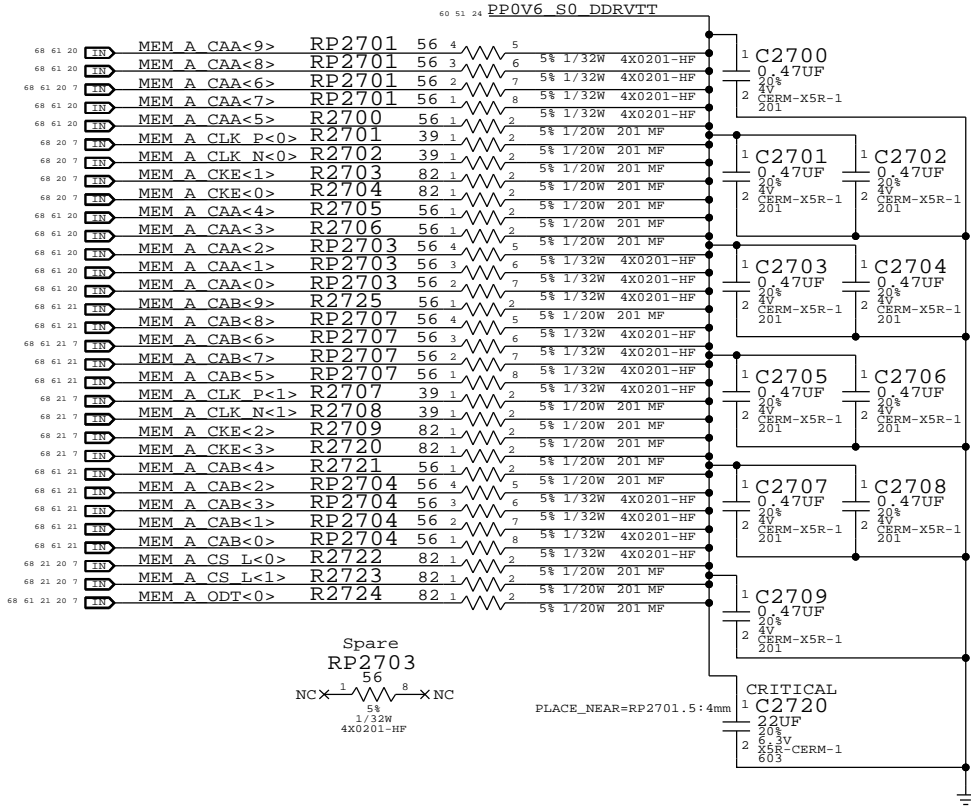
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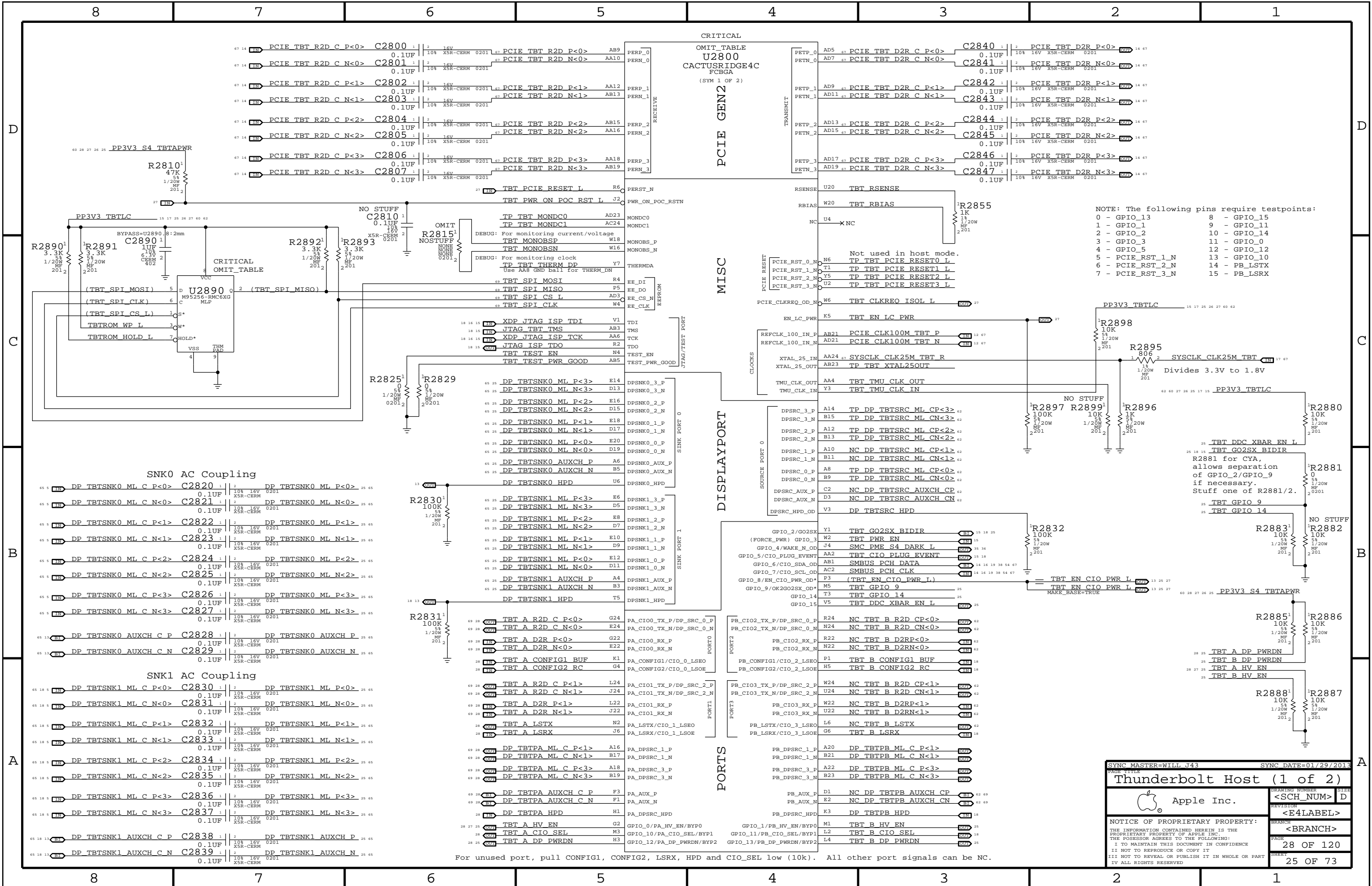
C

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Intel reccommends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC MASTER=WILL J43

SYNC DATE=01/29/2013

Thunderbolt Host (1 of 2)

Apple Inc.

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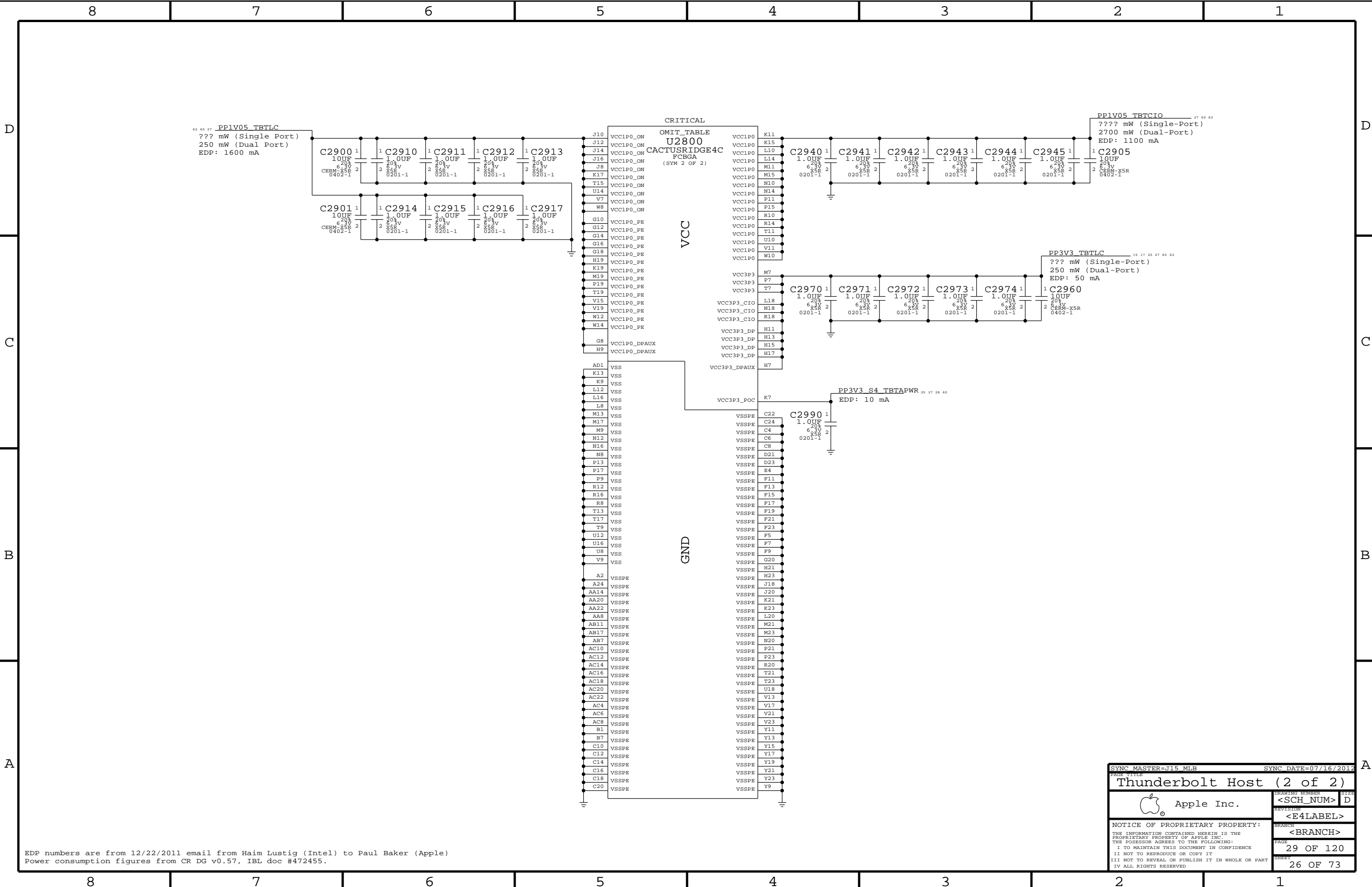
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28 OF 120

SHEET
25 OF 73




EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=J15 MLB

SYNC DATE=07/16/2012

Thunderbolt Host (2 of 2)

 Apple Inc.

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SHEET26 OF 73

Page Notes

Power aliases required by this page:

- PPVIN_SW_TBTBST (8-13V Boost Input)
- PP15V_TBT_REG (15V Boost Output)
- PP3V3_TBT_P3V3TBTFTFET (3.3V FET Input)
- PP3V3_TBT_FET (3.3V FET Output)
- PP3V3_S0_TBTTPWRCTL (3.3V FET Input)
- PP1V05_TBT_P1V05TBTFTFET (1.05V FET Input)
- PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:

- TBT_CLKREQ_L
- TBT_RESET_L

BOM options provided by this page:

(NONE)

TBT 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL
Q3080
SI8409DB

CRITICAL
L3095
6.8UH-4.0A

CRITICAL
D3095
POWERDI-123

PP15V TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

Supervisor & CLKREQ# Isolation

TBT "POC" Power-up Reset

3.3V TBT "LC" Switch

Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max

1.05V TBT "LC" Switch

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ
@ 1.05V	10.4 mOhm Max

1.05V TBT "CIO" Switch

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ
@ 1.05V	10.4 mOhm Max

8	7	6	5	4	3	2	1
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D



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

CRITICAL
L3200
FERR-120-OHM-3A



Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

C

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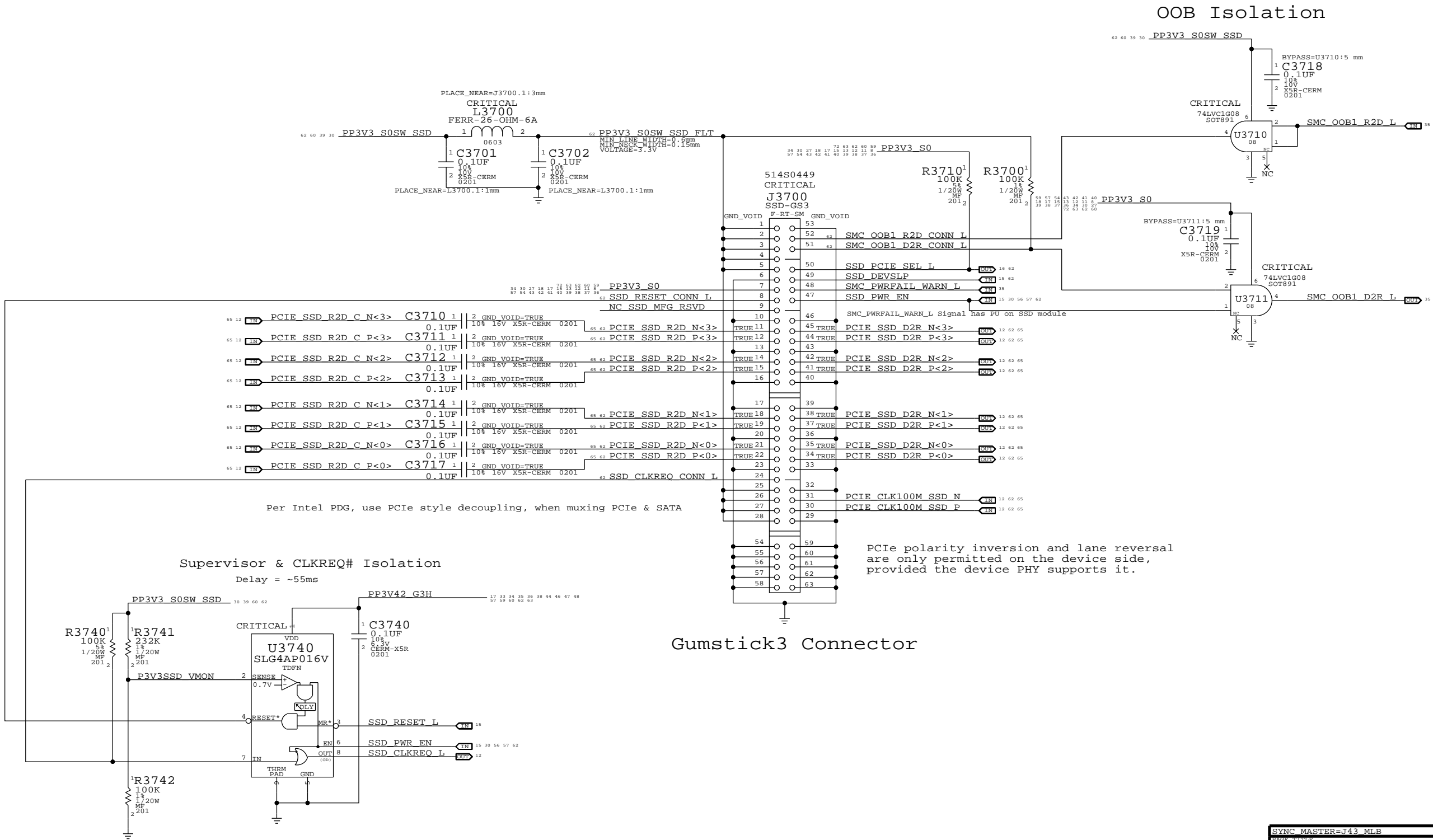
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
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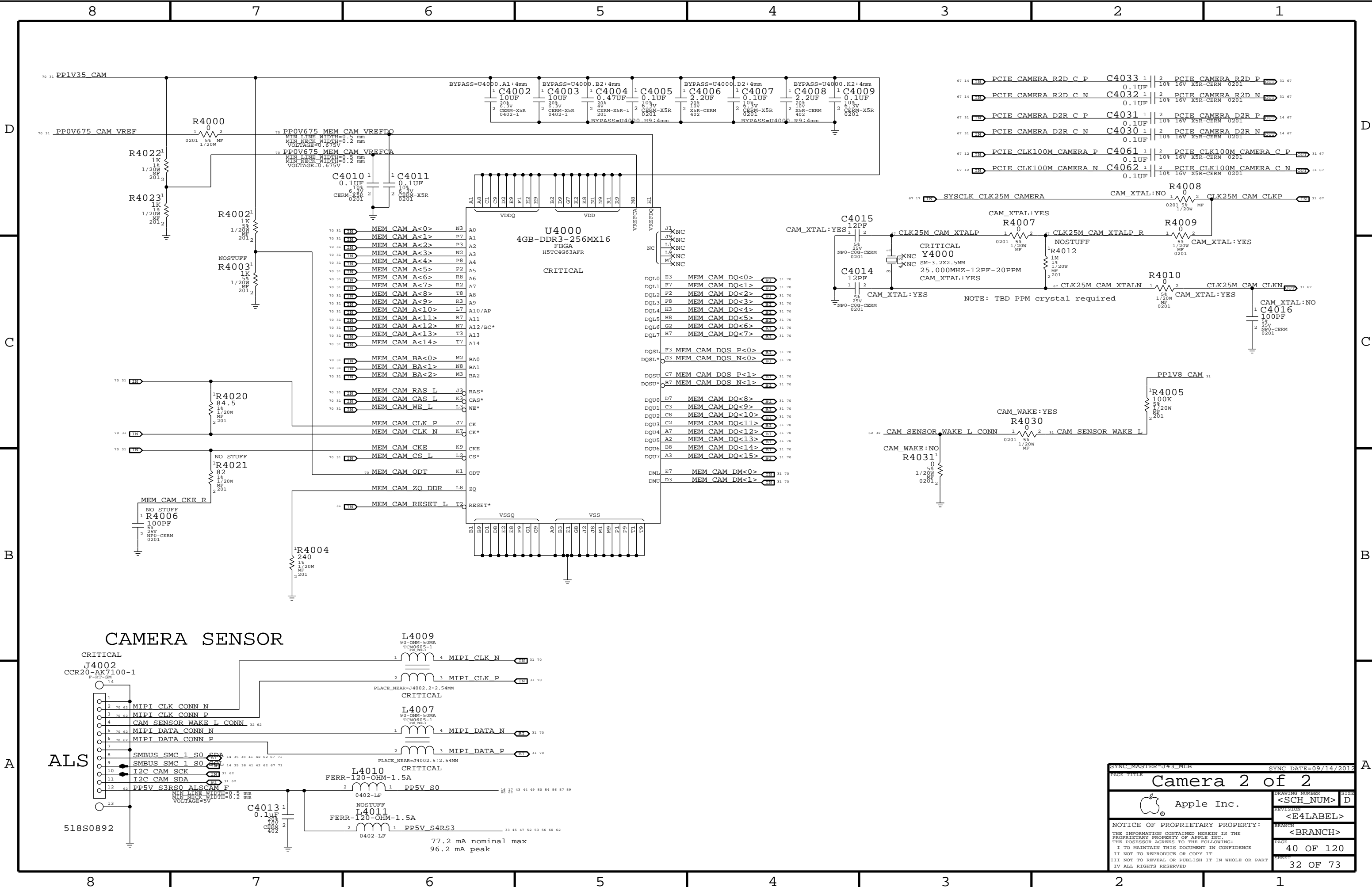
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SYNC MASTER=J43 MLB		SYNC DATE=02/20/2013	
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SSD Connector			
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Camera 2 of 2

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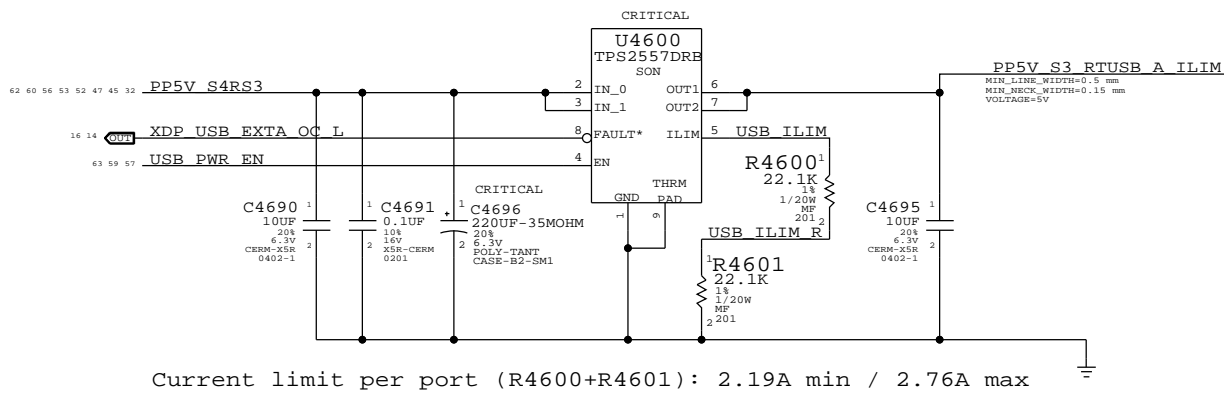
SHEET

32 OF 73

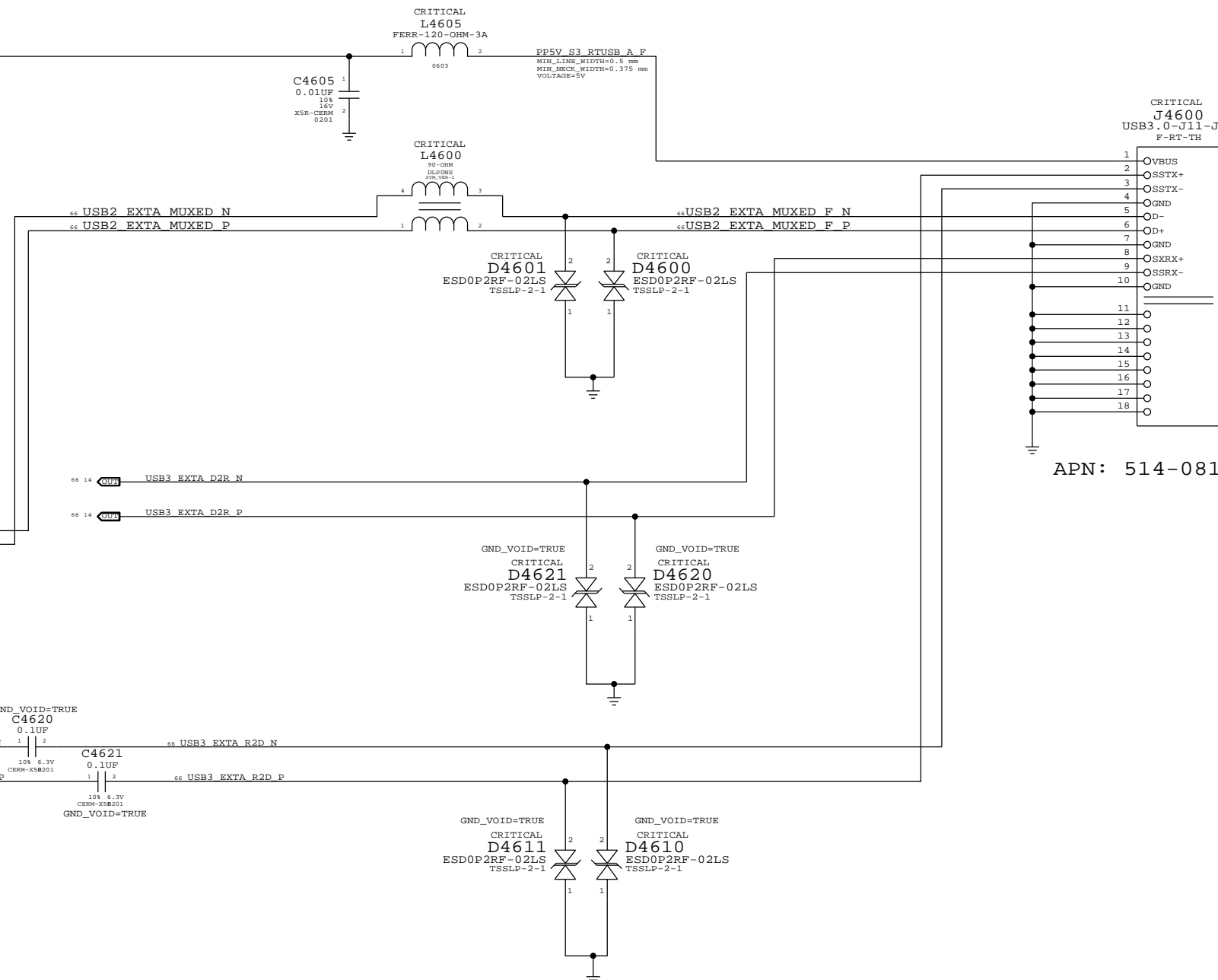
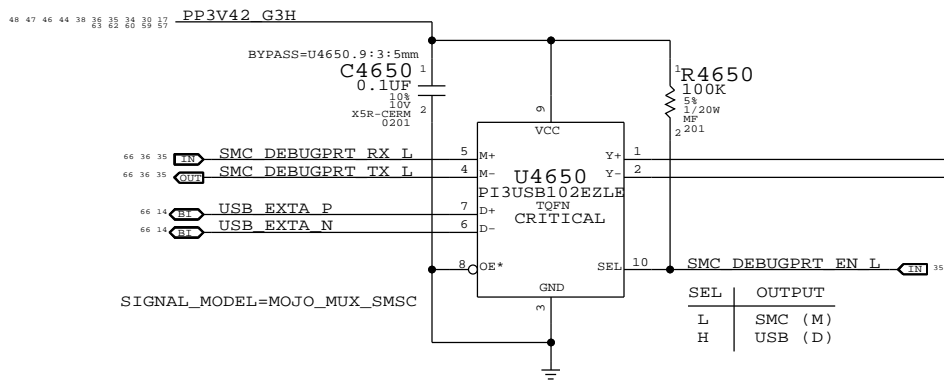
SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012


Right USB Port A

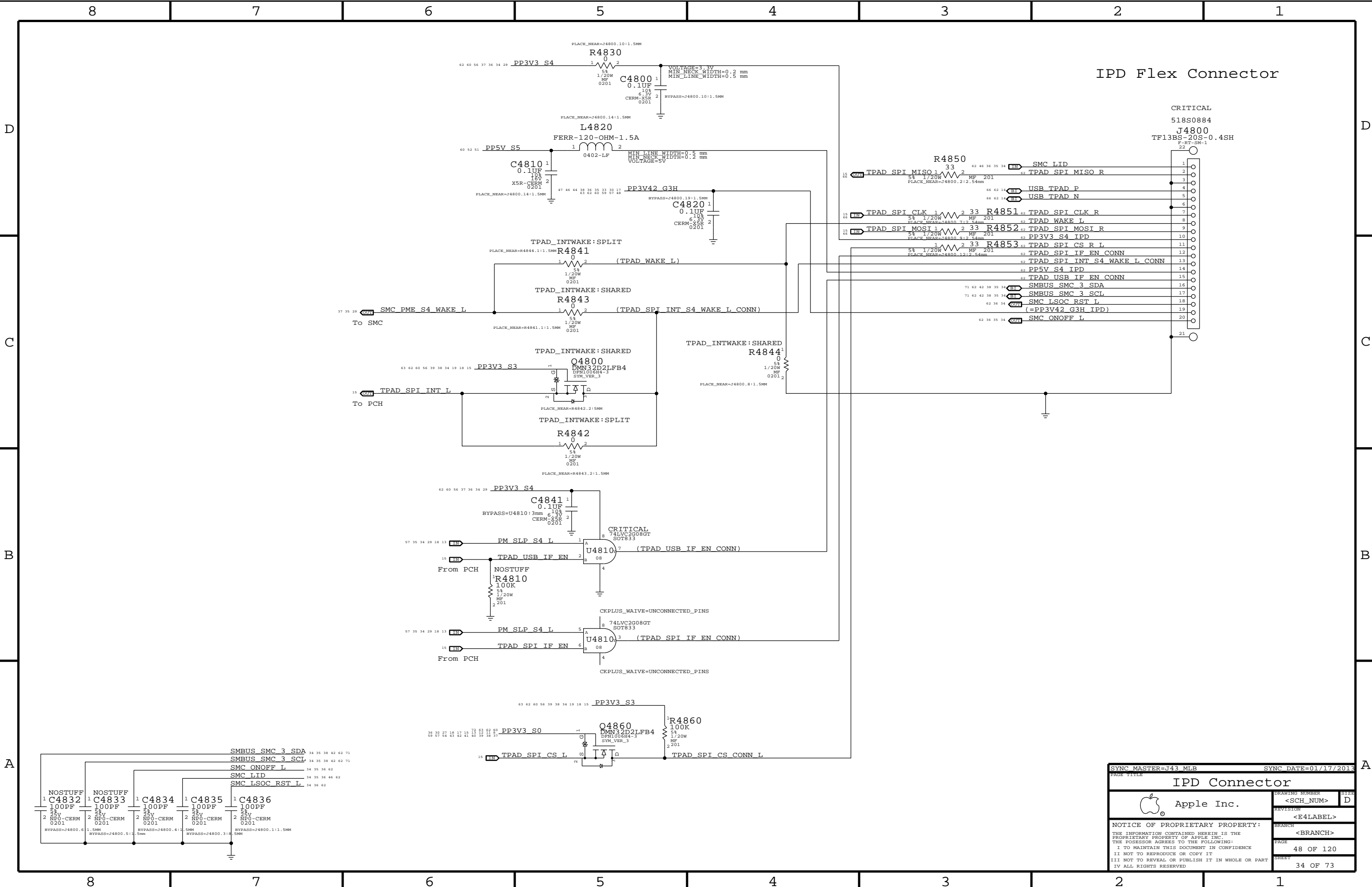
USB Port Power Switch



Mojo SMC Debug Mux




SYNC MASTER=J43 MLB		SYNC DATE=02/20/2013	
PAGE TITLE			
External A USB3 Connector			
 Apple Inc.	DRAWING NUMBER	SIZE	
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	PAGE	46 OF 120	
	SHEET	33 OF 73	

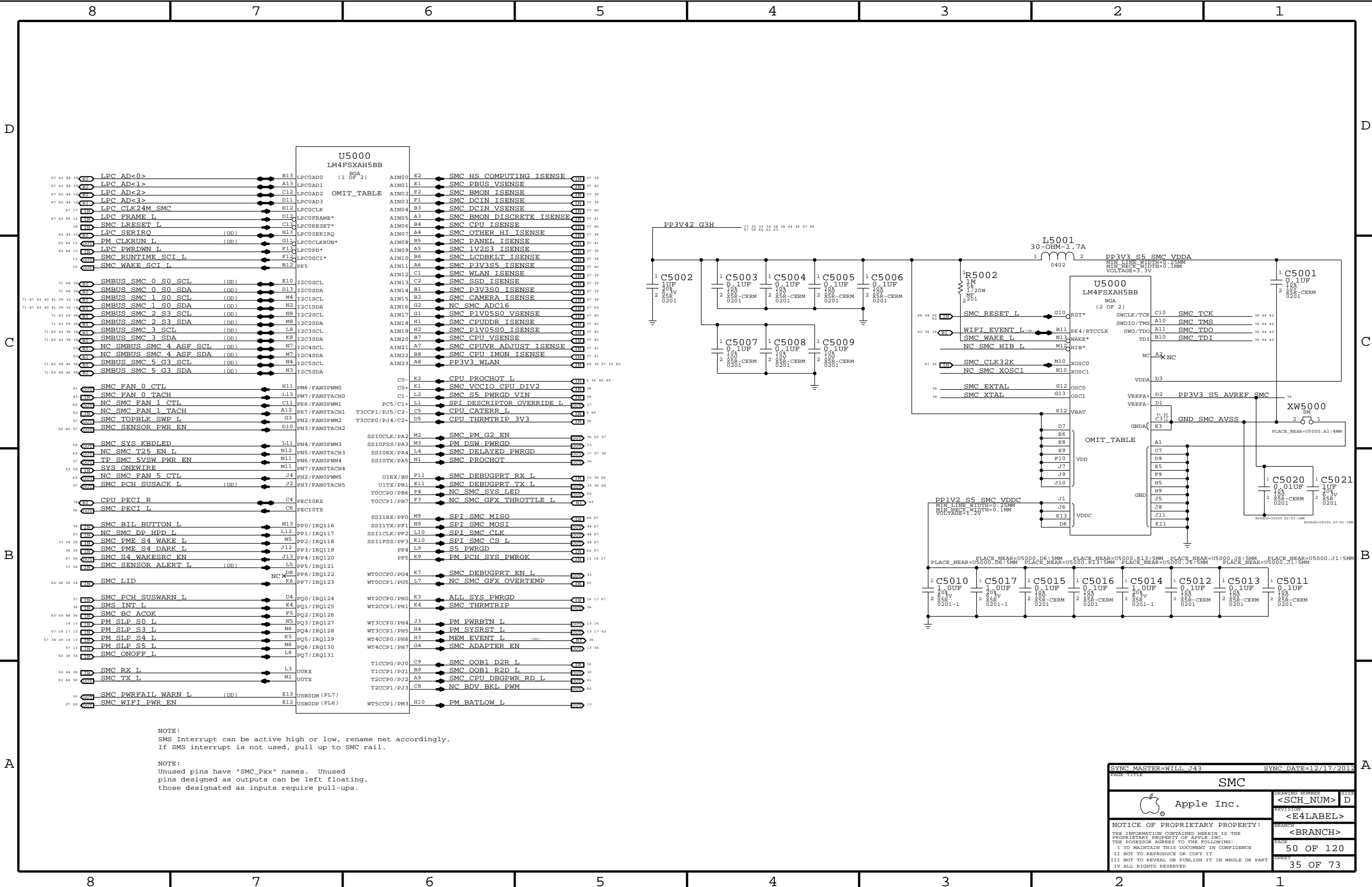


IPD Flex Connector

CRITICAL	
518S0884	
J4800	
TF13BS-20S-0.4SH	
F-RT-SM-1	
22	
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TPAD SPI MISO L	TPAD SPI MISO R
USB TPAD P	USB TPAD N
TPAD SPI CLK L	TPAD SPI CLK R
TPAD WAKE L	TPAD SPI MOSI R
TPAD SPI MOSI L	TPAD SPI MOSI R
TPAD SPI CS L	TPAD SPI CS R
TPAD SPI IF EN CONN	TPAD SPI INT S4 WAKE L CONN
TPAD USB IF EN CONN	PP5V S4 IPD
SMBUS SMC 3 SDA	SMBUS SMC 3 SCL
SMC LSOC RST L	(=PP3V42_G3H IPD)
SMC ONOFF L	

SYNC MASTER=J43 MLB		SYNC DATE=01/17/2013	
PAGE TITLE			
IPD Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		<BRANCH>	
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NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=WILL J43		SYNC DATE=12/17/2012	
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SMC		DRAWING NUMBER	
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		35 OF 73	

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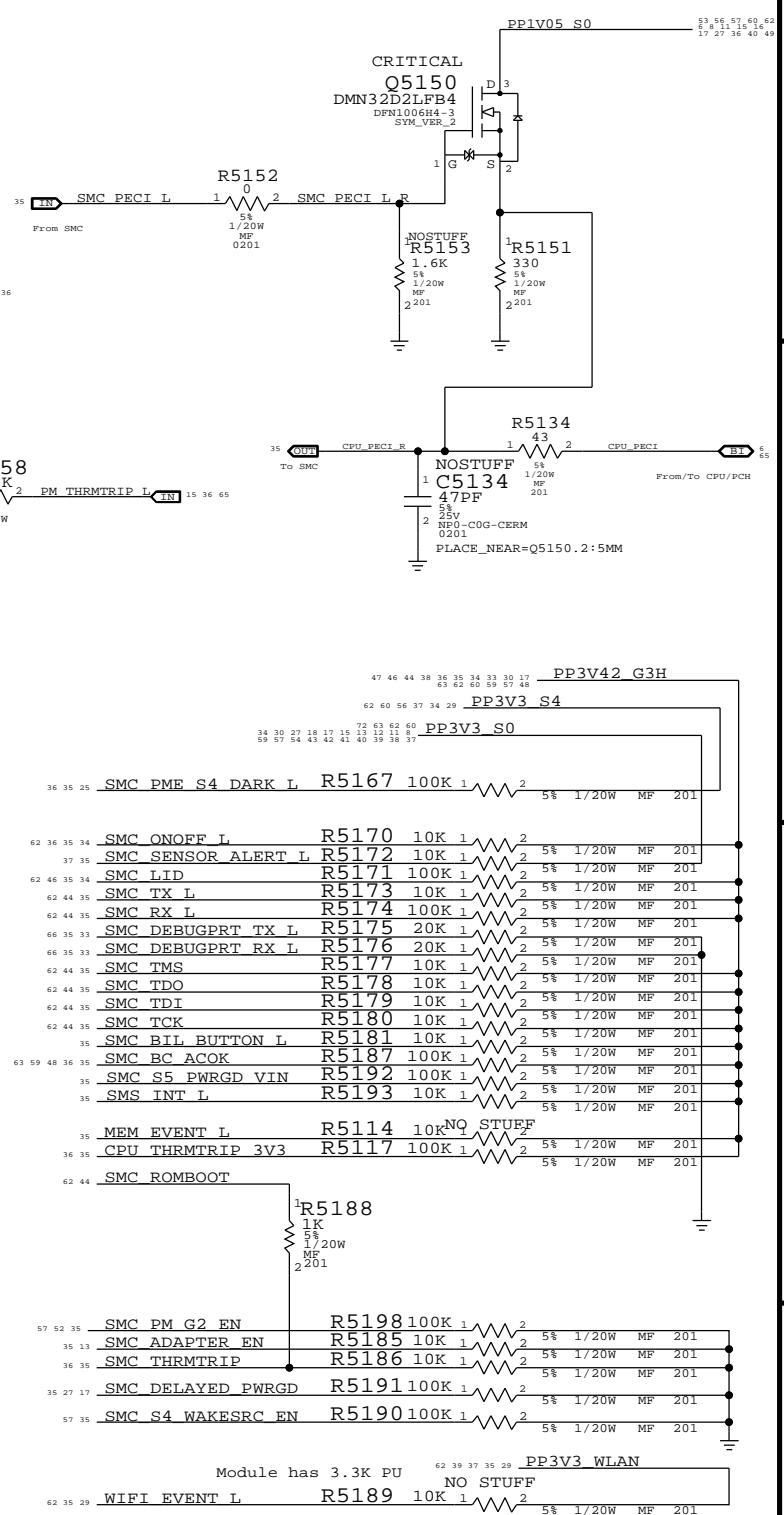
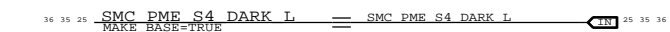
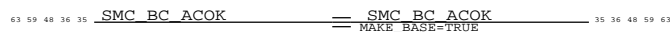


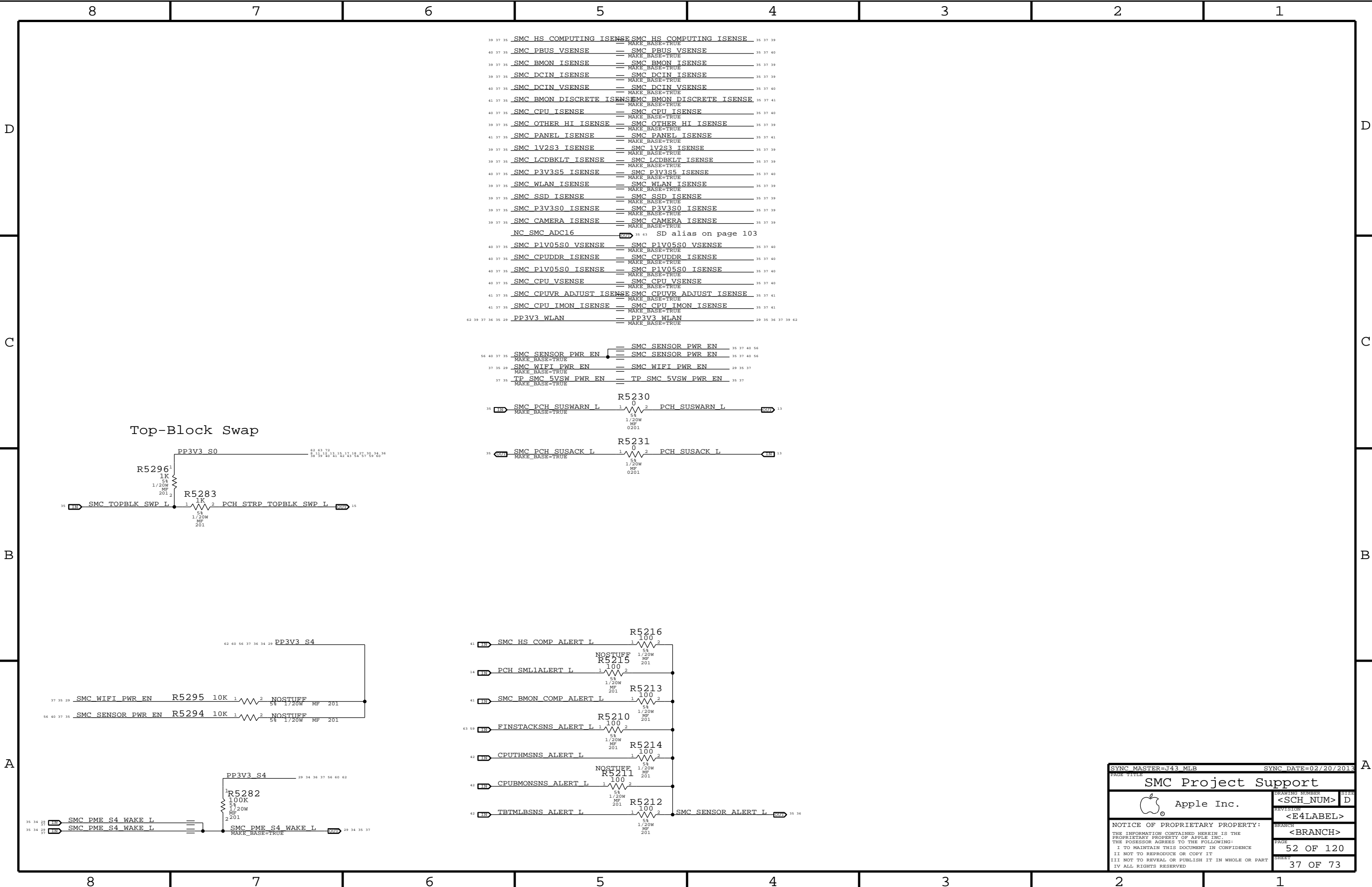
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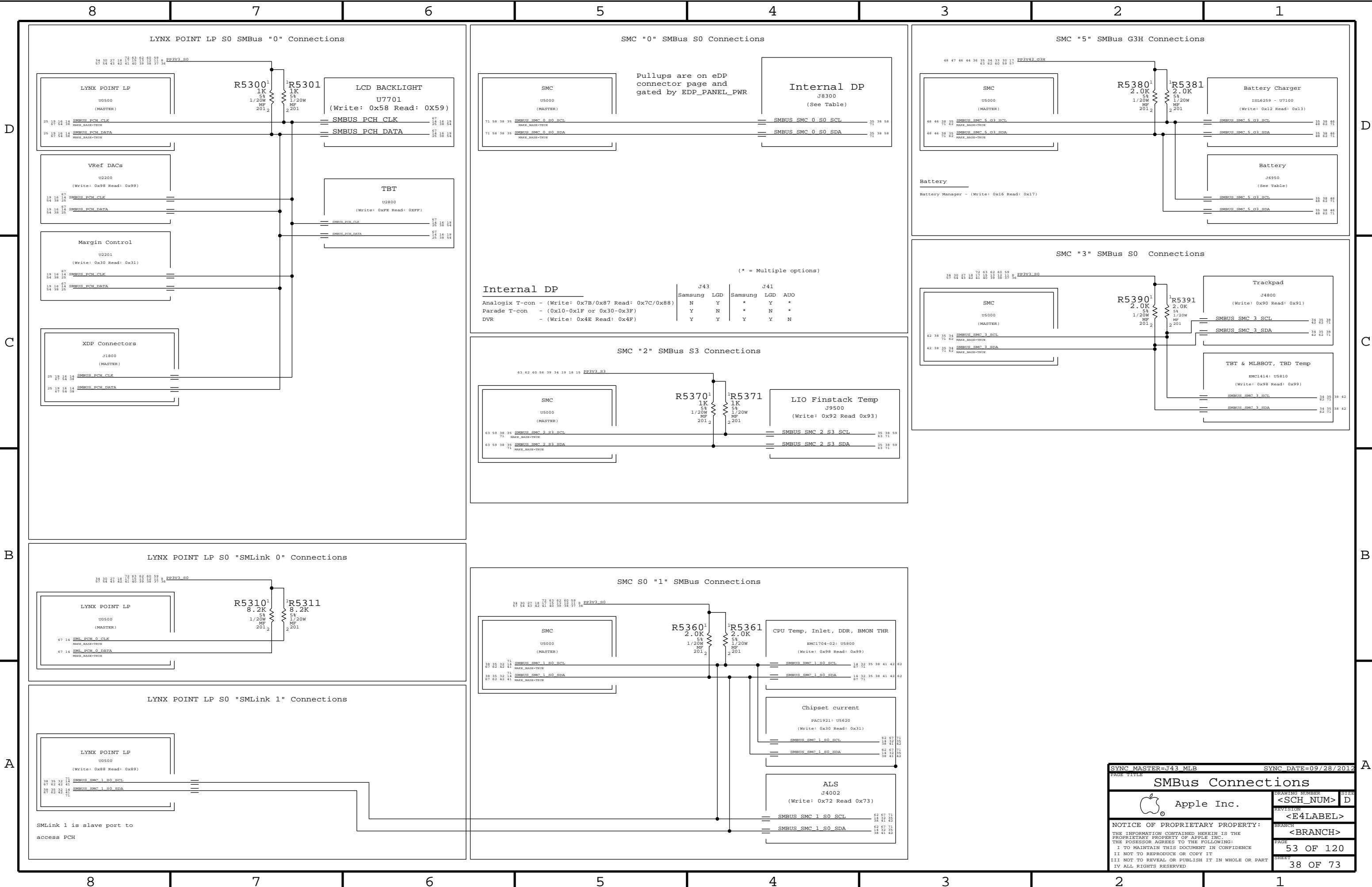
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D






SYNC MASTER=J43 MLB

SYNC DATE=09/28/2012

SMBus Connections

 Apple Inc.

DRAWING NUMBER
<SCH_NUM> D

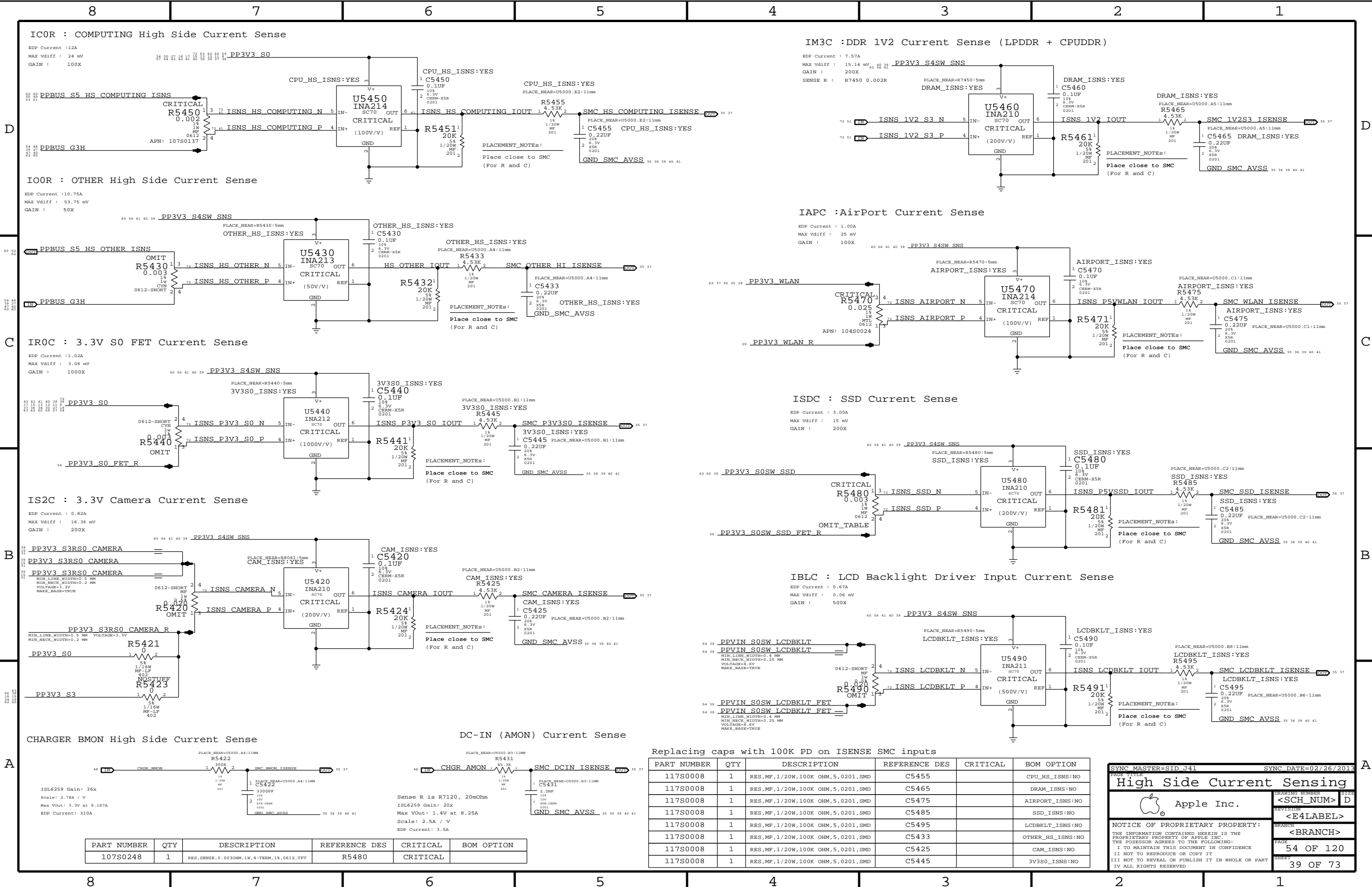
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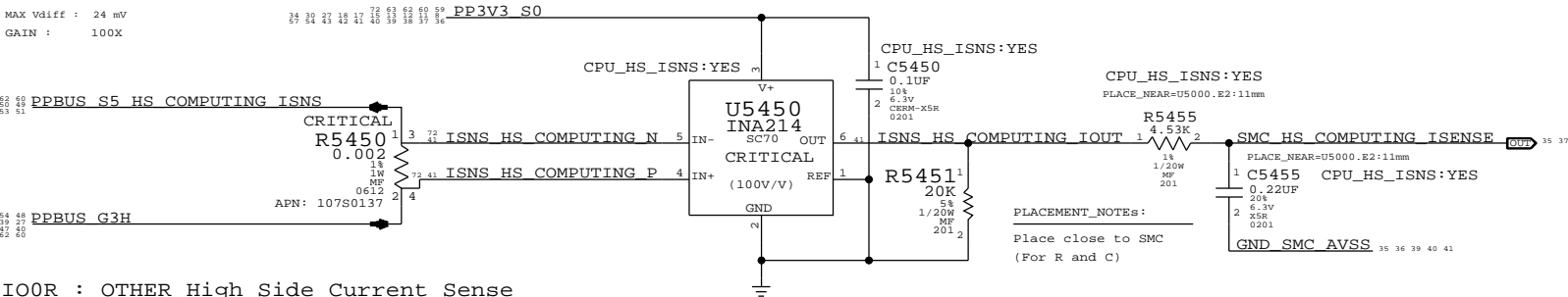
PAGE
53 OF 120

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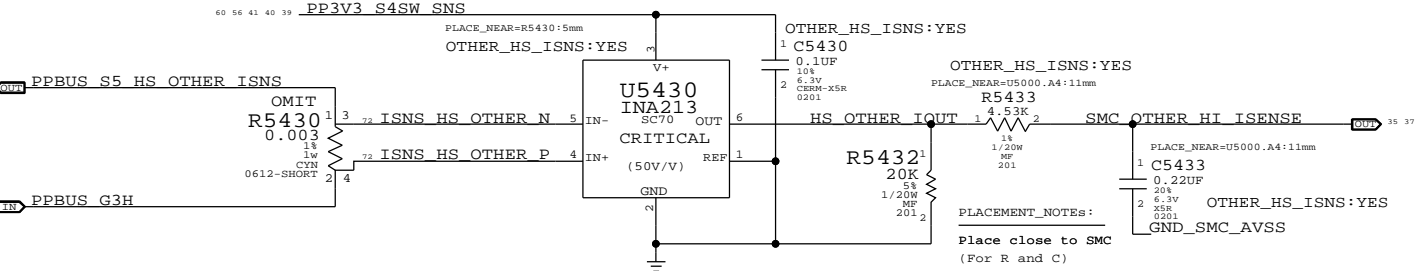
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



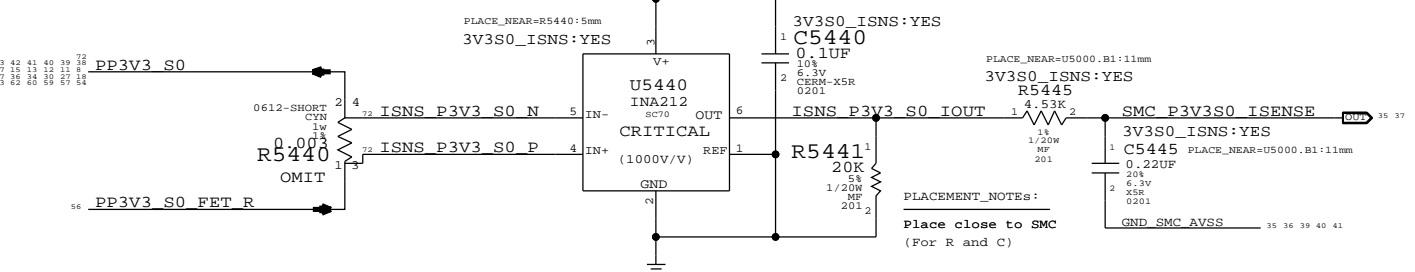
IO0R : OTHER High Side Current Sense

EDP Current :10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X



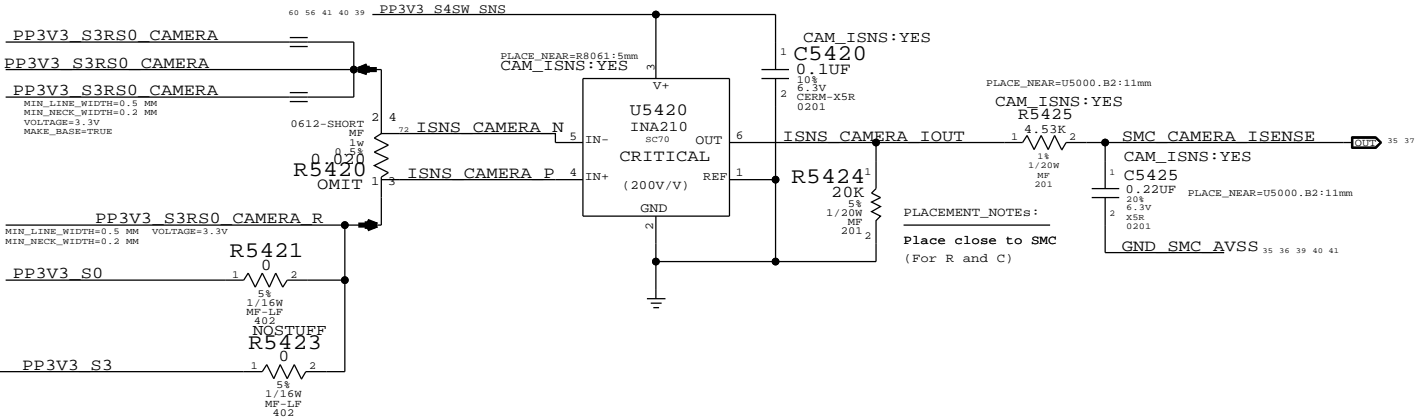
IR0C : 3.3V S0 FET Current Sense

EDP Current :1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X

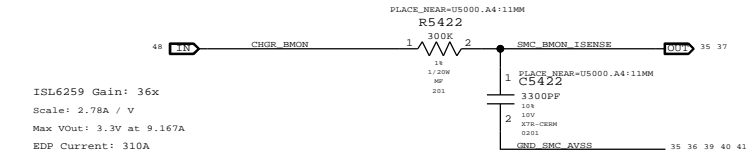


IS2C : 3.3V Camera Current Sense

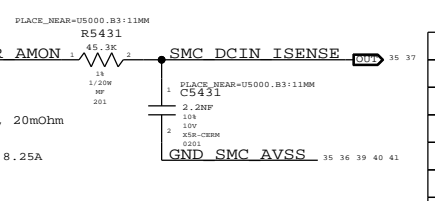
EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X



CHARGER BMON High Side Current Sense

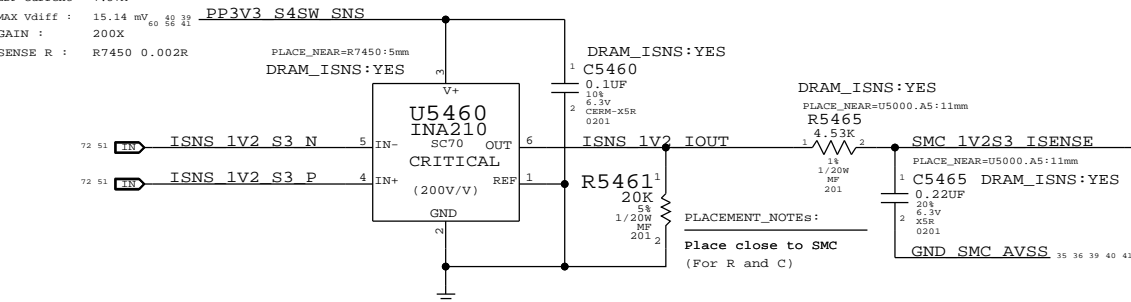


DC-IN (AMON) Current Sense



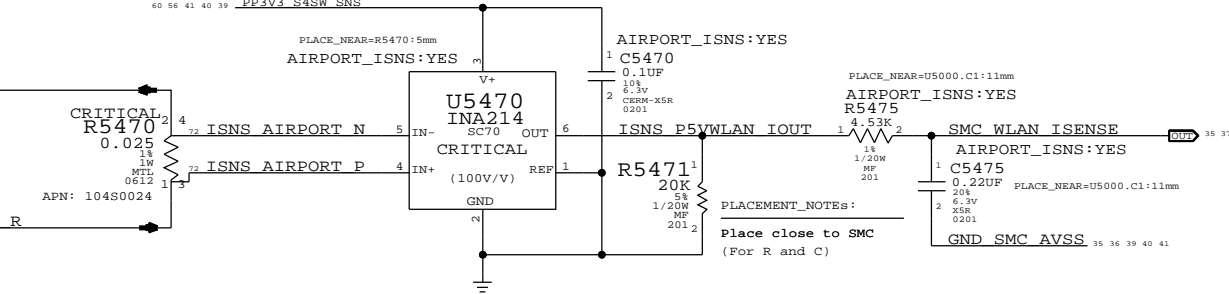
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R



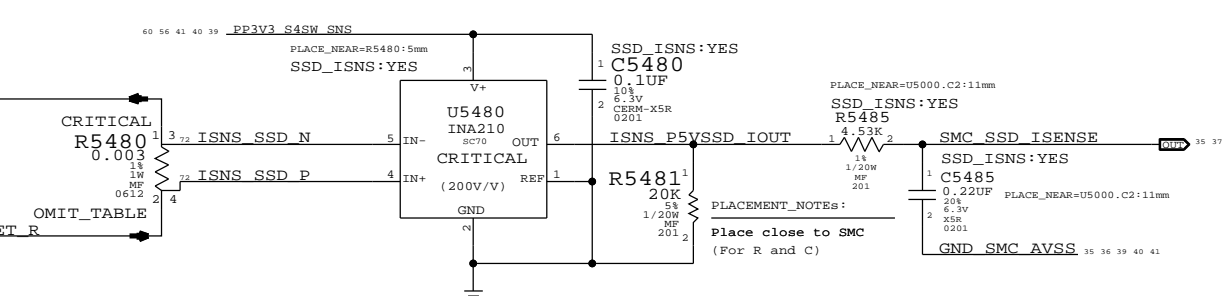
IAPC :AirPort Current Sense

EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X



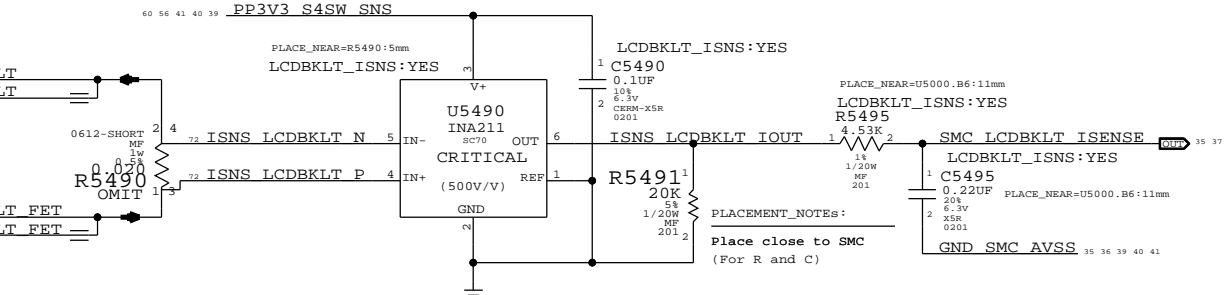
ISDC : SSD Current Sense

EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X



IBLC : LCD Backlight Driver Input Current Sense

EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC MASTER=SID_141

SYNC DATE=02/26/2013

High Side Current Sensing

Apple Inc.

DRAWING NUMBER

SIZE

<SCH_NUM>

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REVISION

<E4LABEL>

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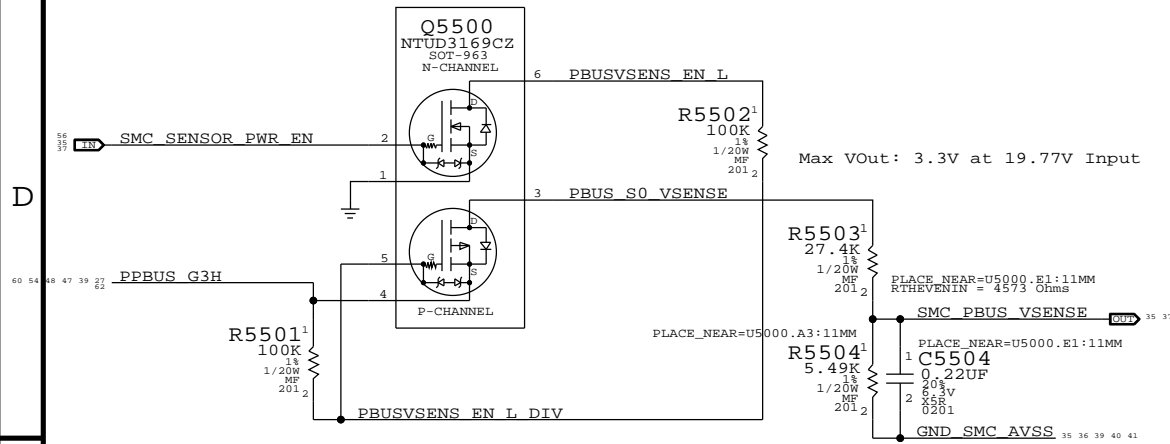
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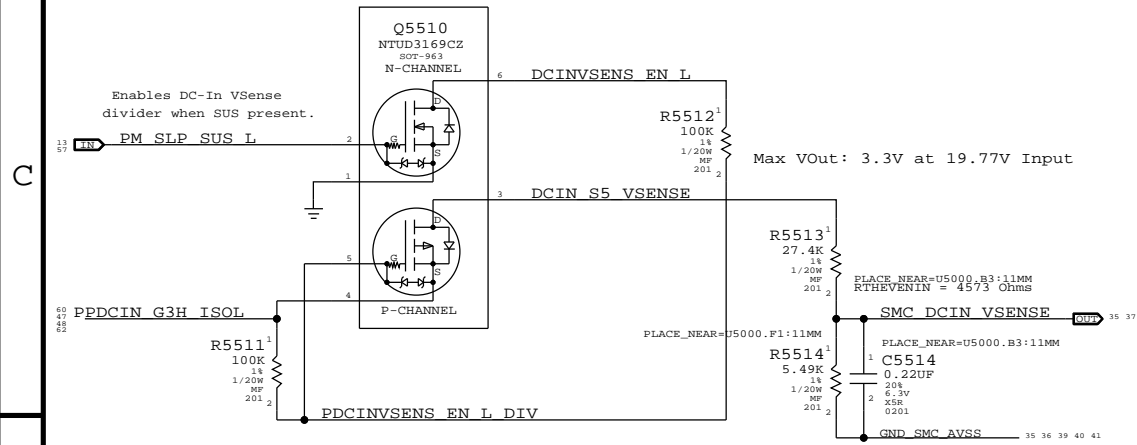
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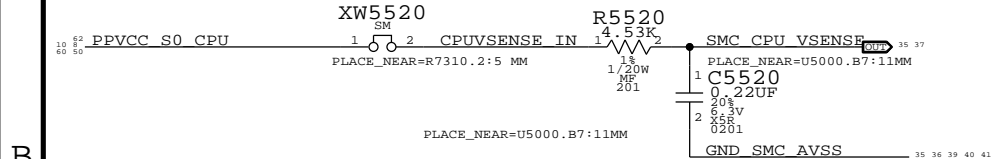
VP0R: PBUS Voltage Sense Enable & Filter



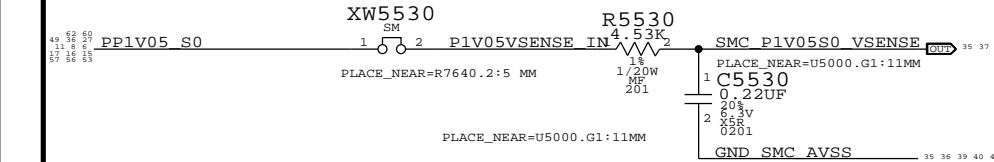
VD0R: DC-In Voltage Sense Enable & Filter



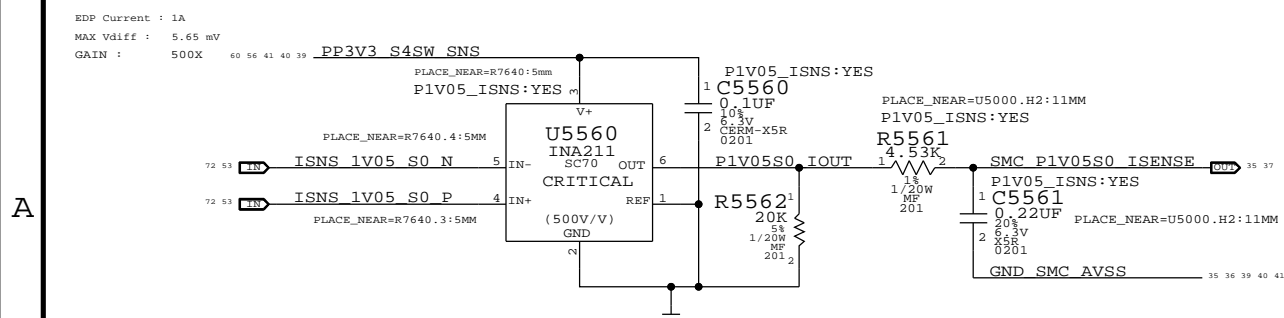
CPU Vcore Voltage Sense / Filter



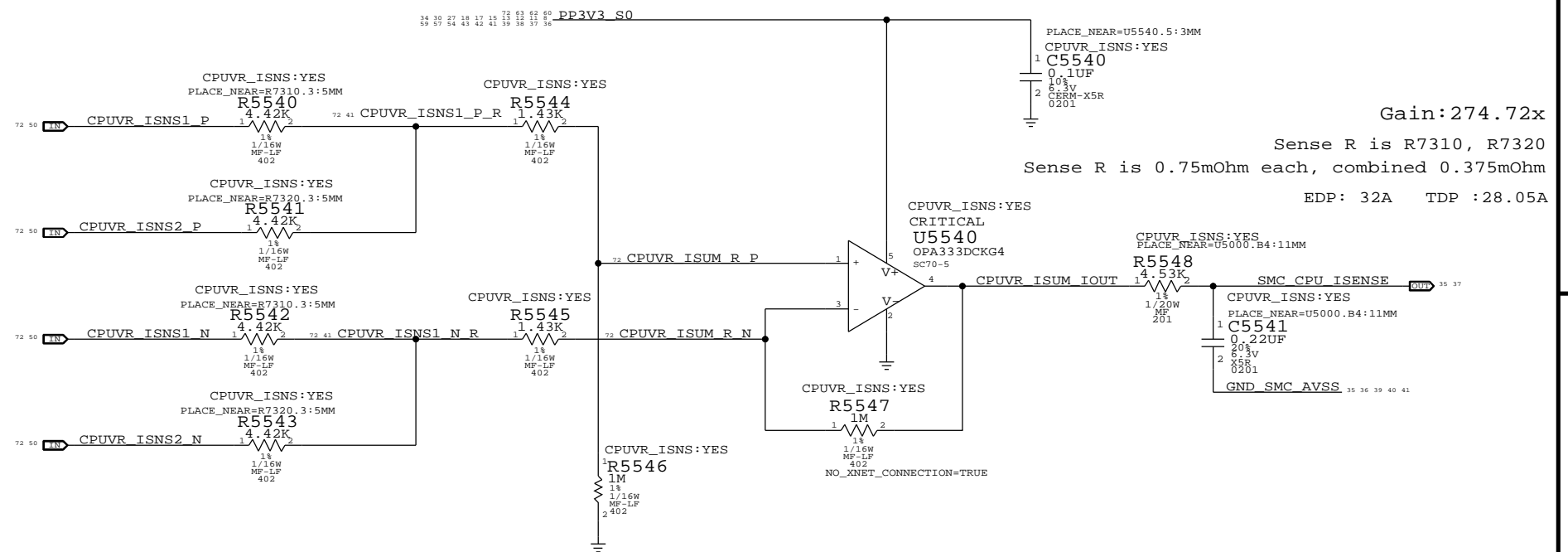
1.05V Voltage Sense / Filter



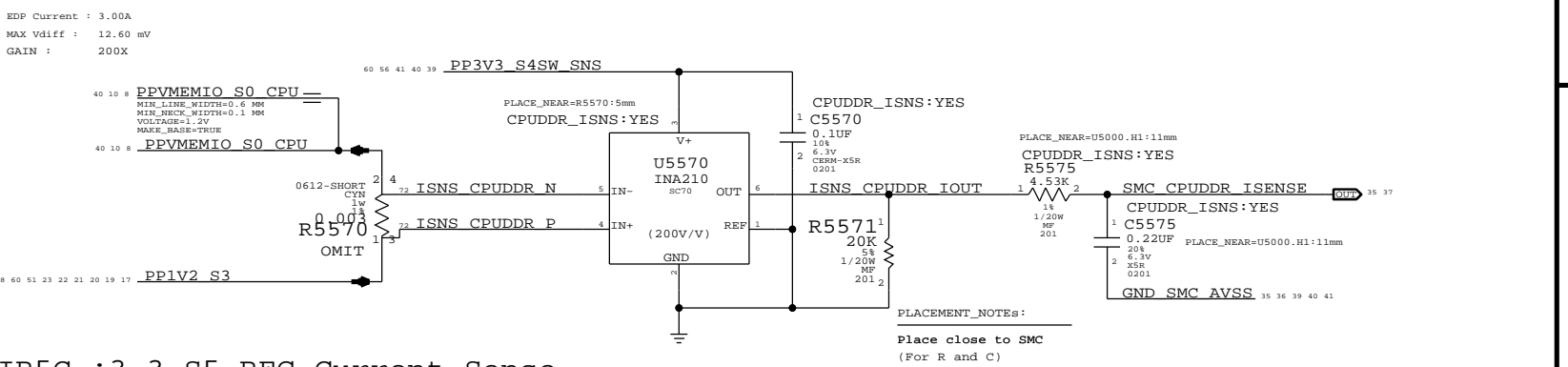
IC1C: 1.05V S0 CURRENT SENSE / FILTER



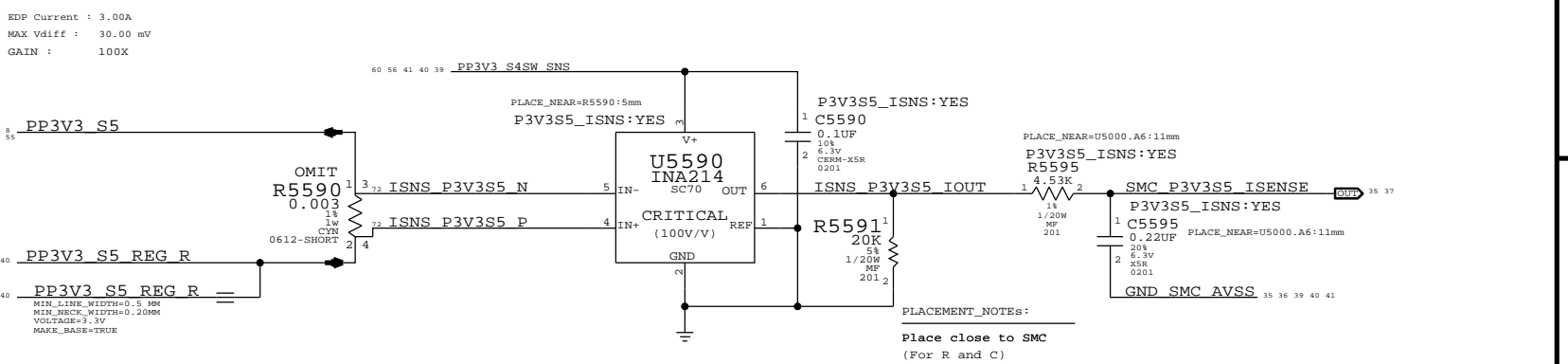
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense

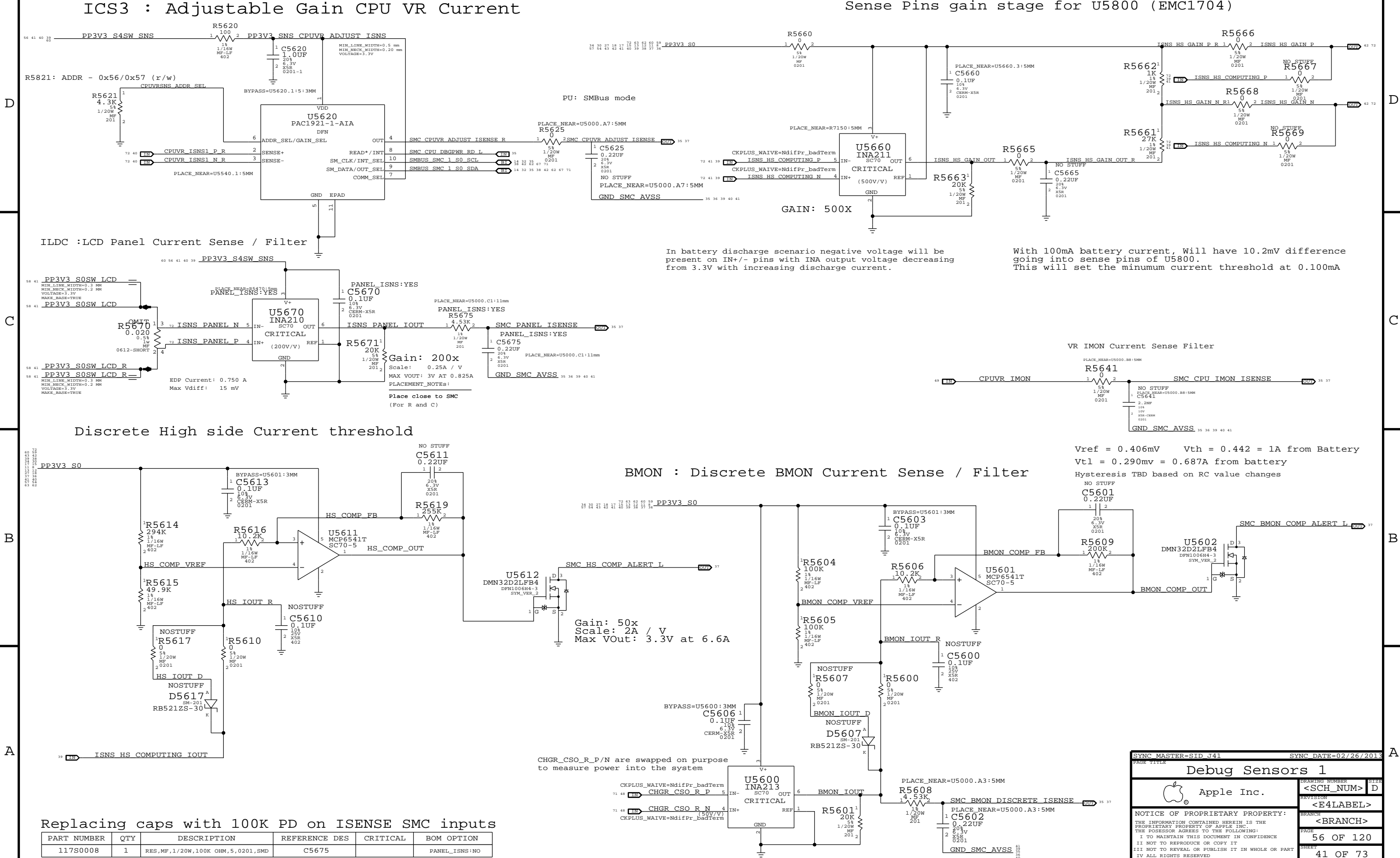


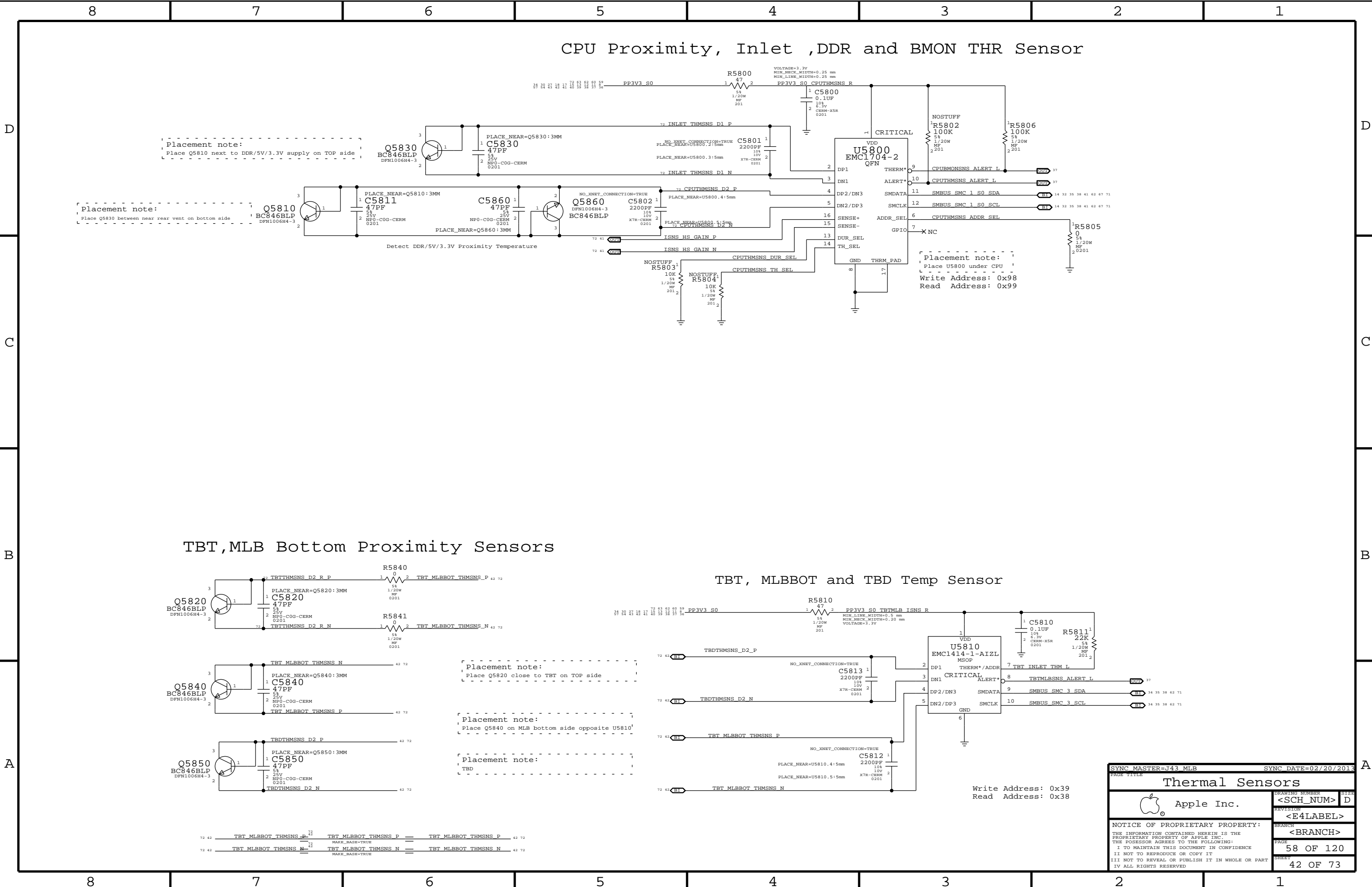
Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

Voltage & Load Side Current Sensing

SYNC MASTER=SID_J41		SYNC DATE=02/26/2013	
Apple Inc.		<SCH_NUM> D	
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Placement note:
Place Q5810 next to DDR/5V/3.3V supply on TOP side

Placement note:
Place Q5830 between near rear vent on bottom side

Placement note:
Place U5800 under CPU
Write Address: 0x98
Read Address: 0x99

TBT, MLB Bottom Proximity Sensors

TBT, MLBBOT and TBD Temp Sensor

Placement note:
Place Q5820 close to TBT on TOP side

Placement note:
Place Q5840 on MLB bottom side opposite U5810

Placement note:
TBD

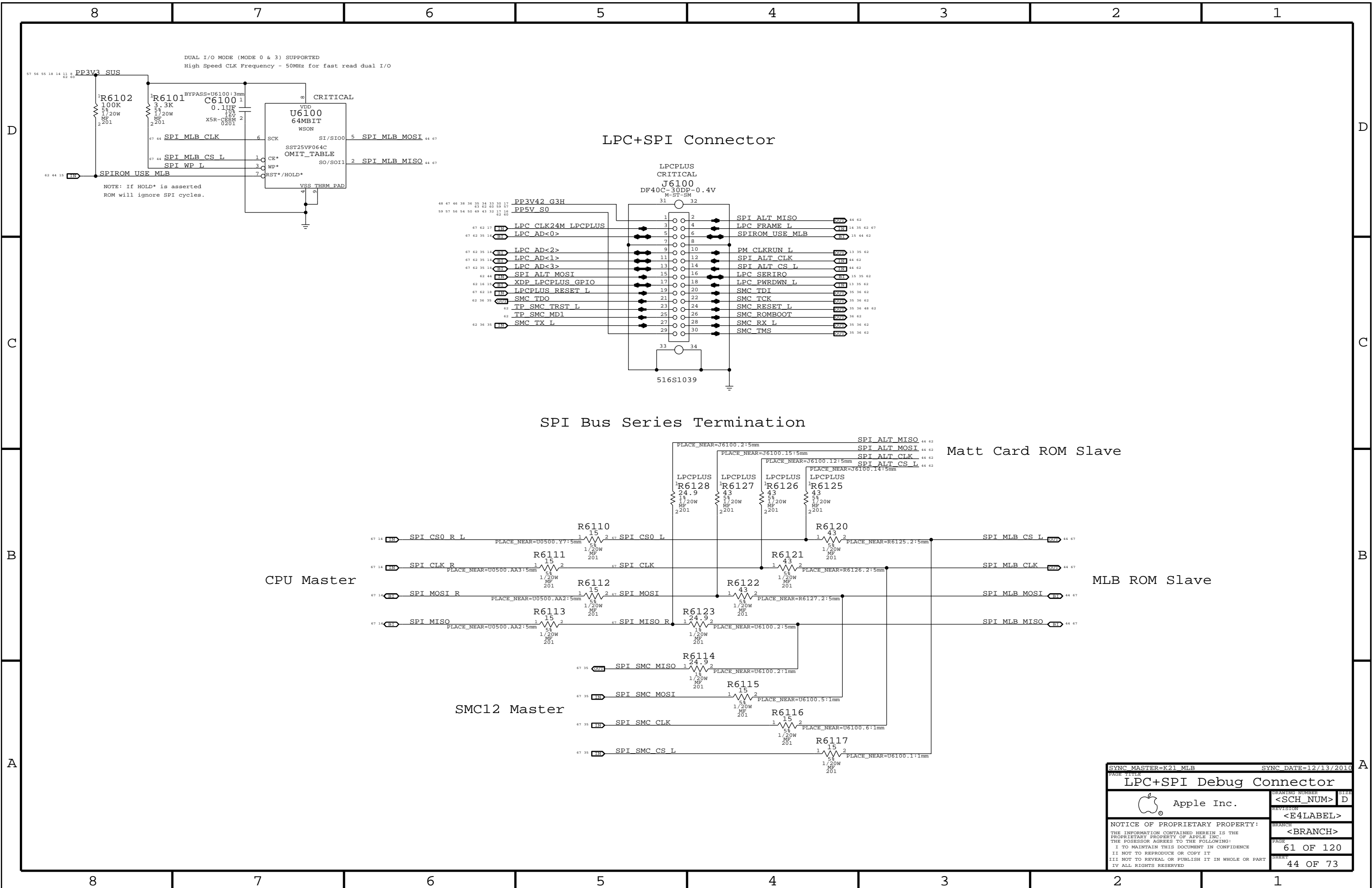
Write Address: 0x39
Read Address: 0x38


TBT MLBBOT THMSNS P	TBT MLBBOT THMSNS P	TBT MLBBOT THMSNS P
TBT MLBBOT THMSNS N	TBT MLBBOT THMSNS N	TBT MLBBOT THMSNS N

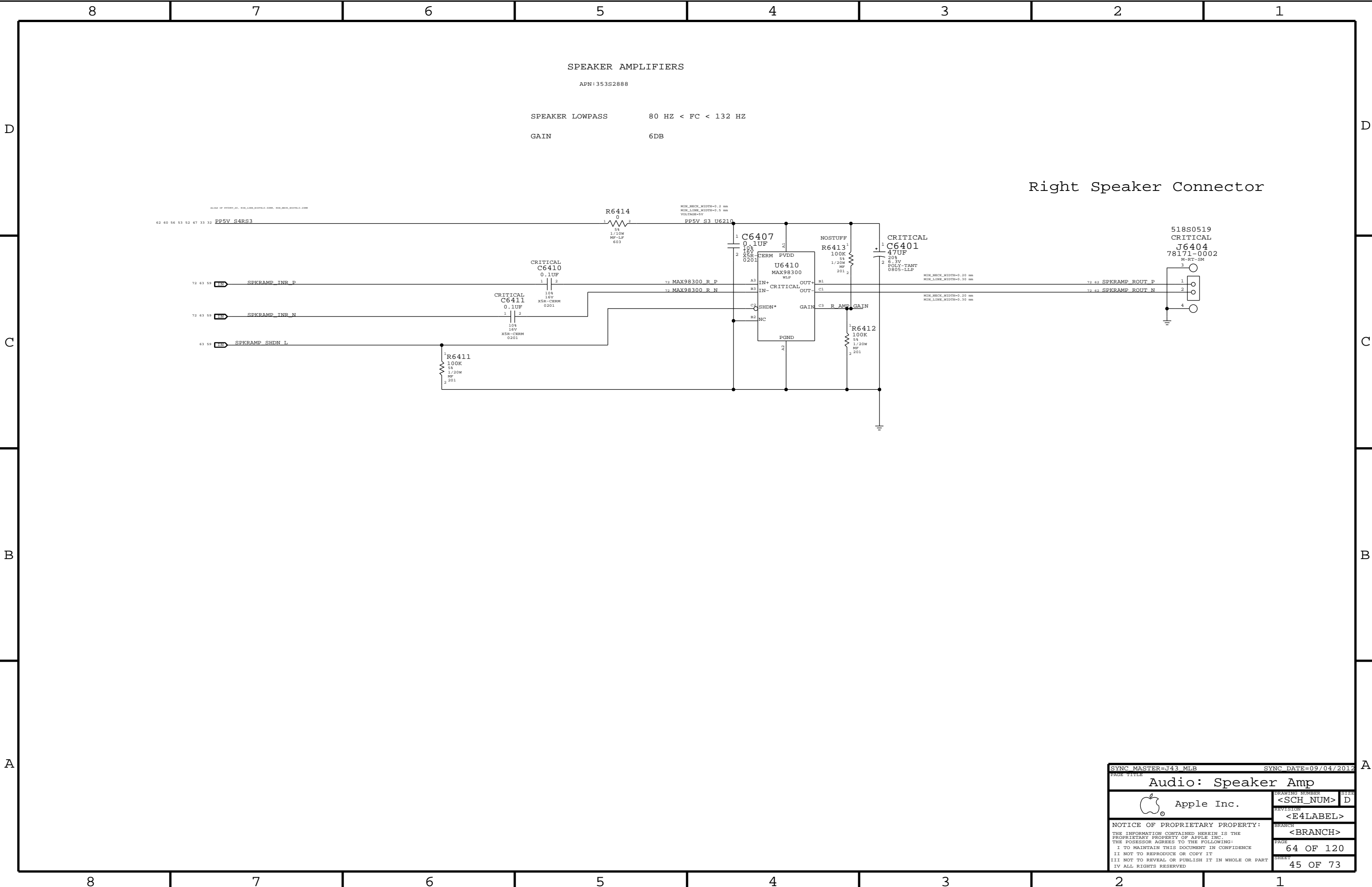
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Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		PAGE	58 OF 120
		SHEET	42 OF 73
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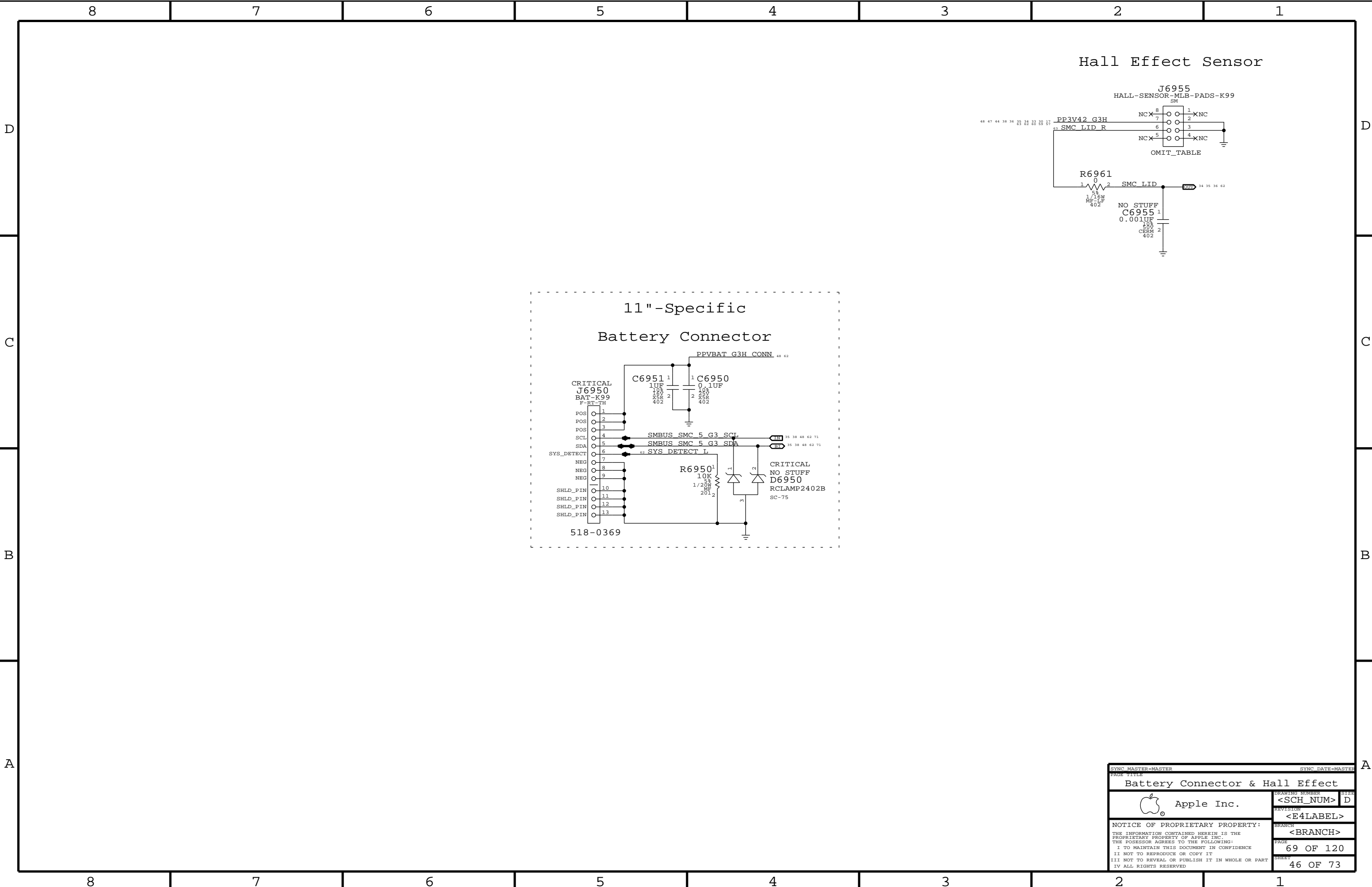
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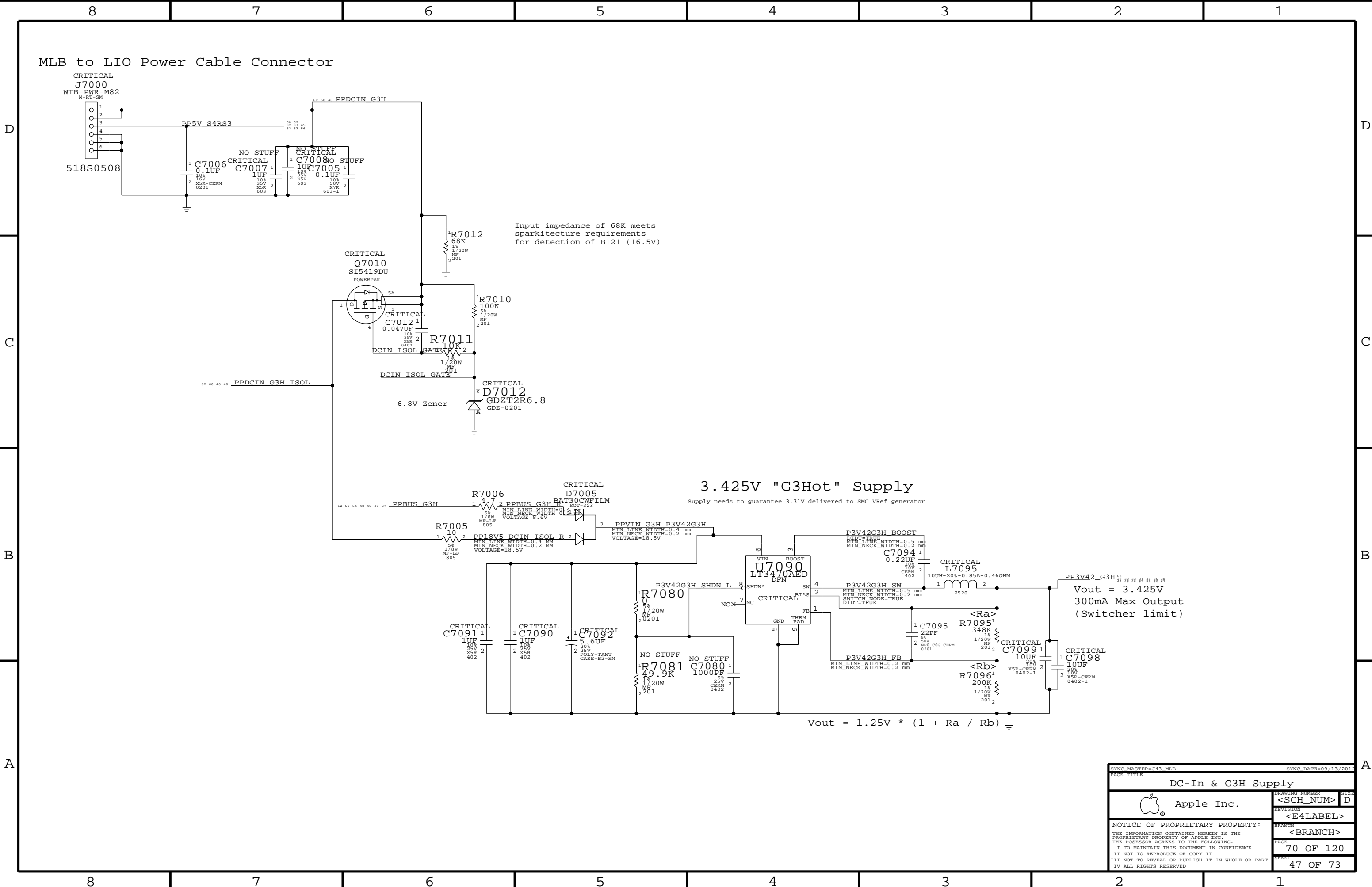
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SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
PAGE TITLE			
LPC+SPI Debug Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
	REVISION		
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SHEET		44 OF 73	








Input impedance of 68K meets sparkiterture requirements for detection of B121 (16.5V)

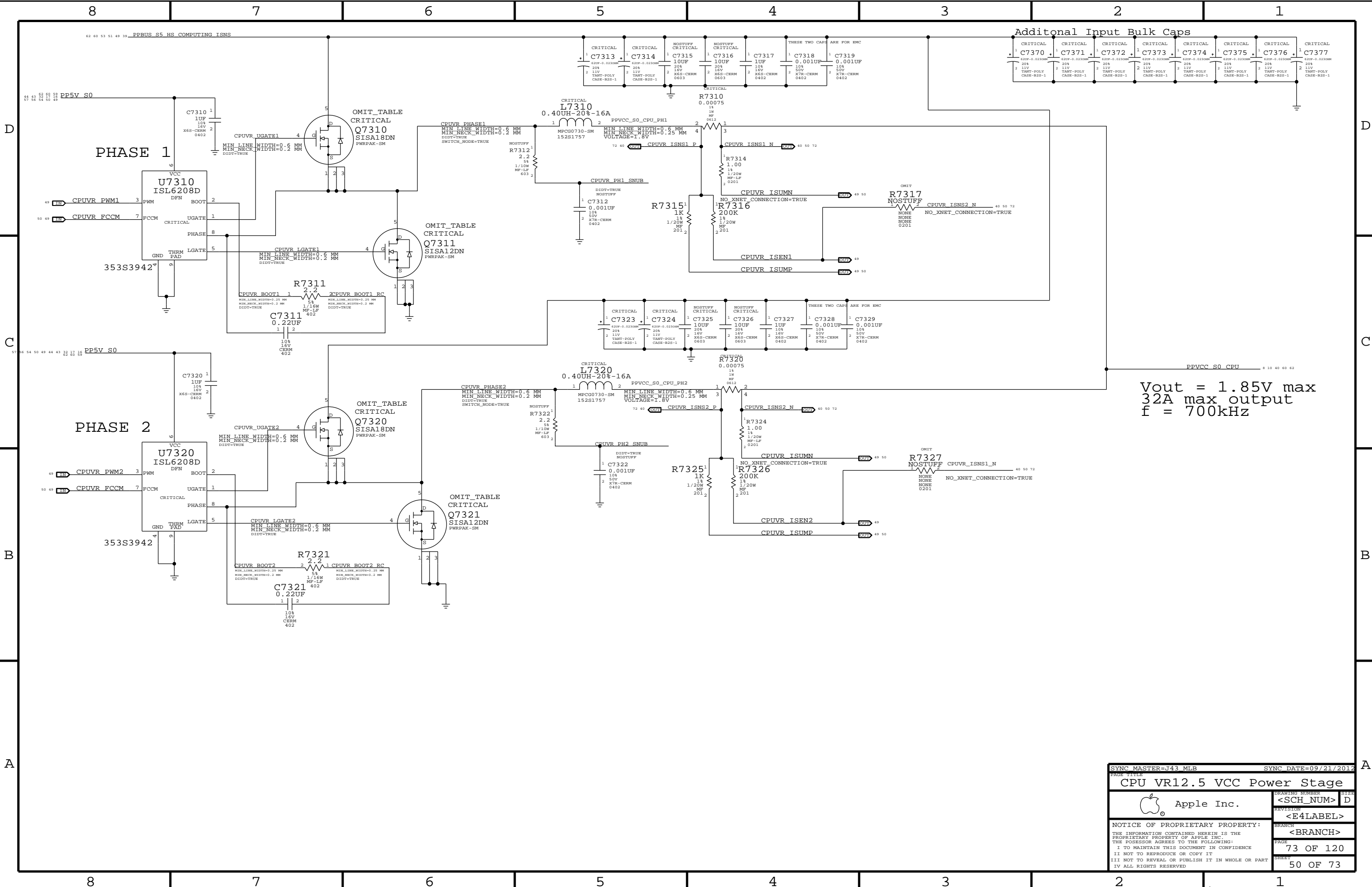
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 3.425V
300mA Max Output
(Switcher limit)


$$Vout = 1.25V * (1 + Ra / Rb)$$

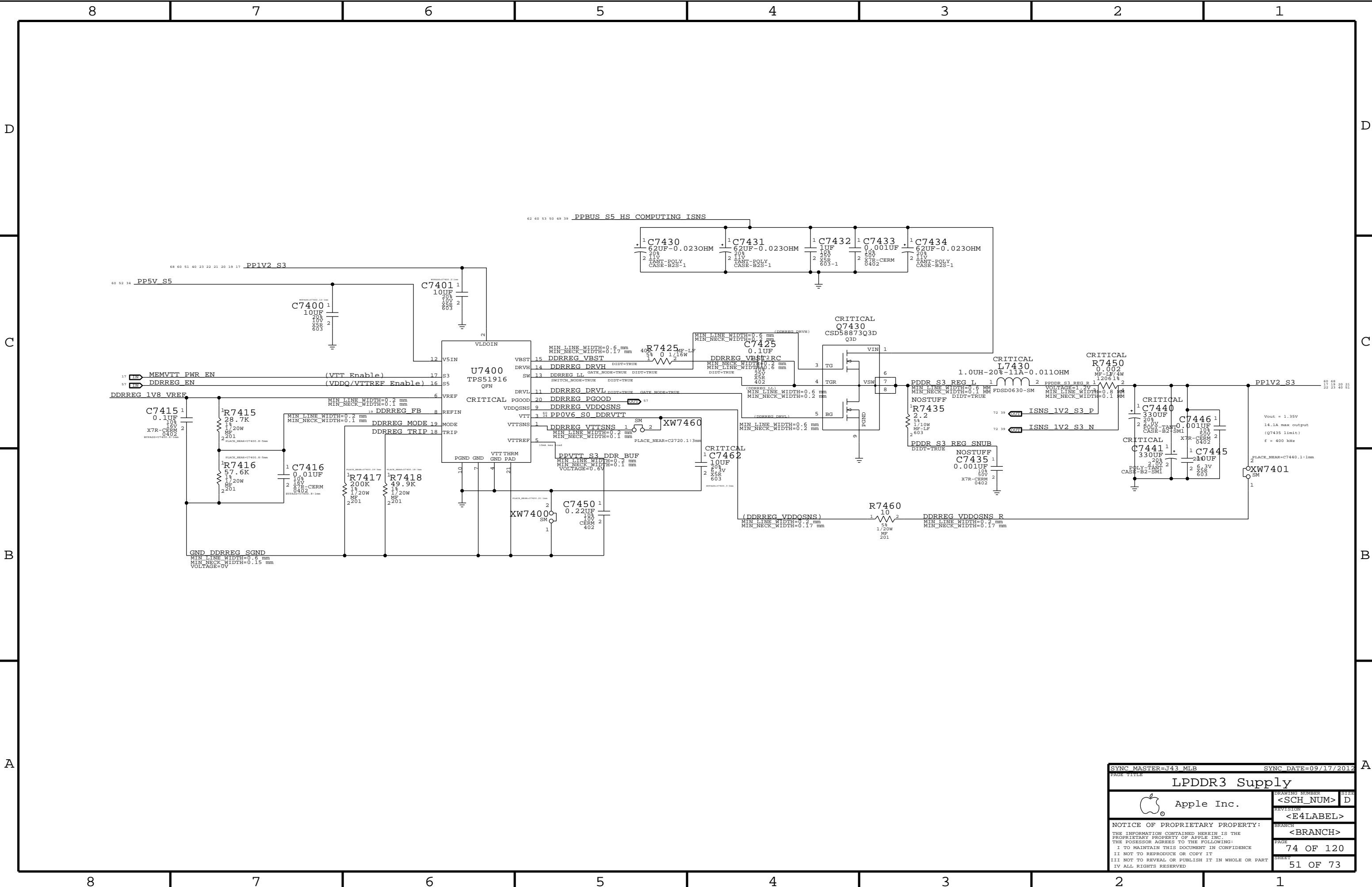
SYNC MASTER=J43 MLB		SYNC DATE=09/13/2012	
PAGE TITLE			
DC-In & G3H Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
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Vout = 1.85V max
32A max output
f = 700kHz

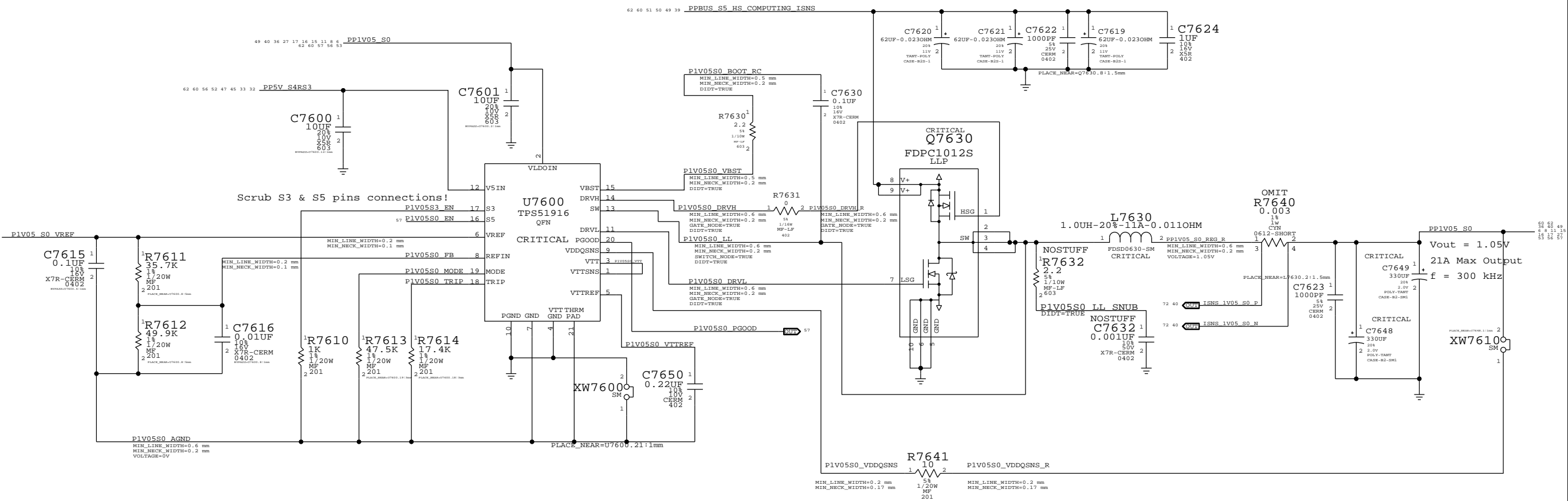
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PAGE TITLE			
CPU VR12.5 VCC Power Stage			
		Apple Inc.	
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


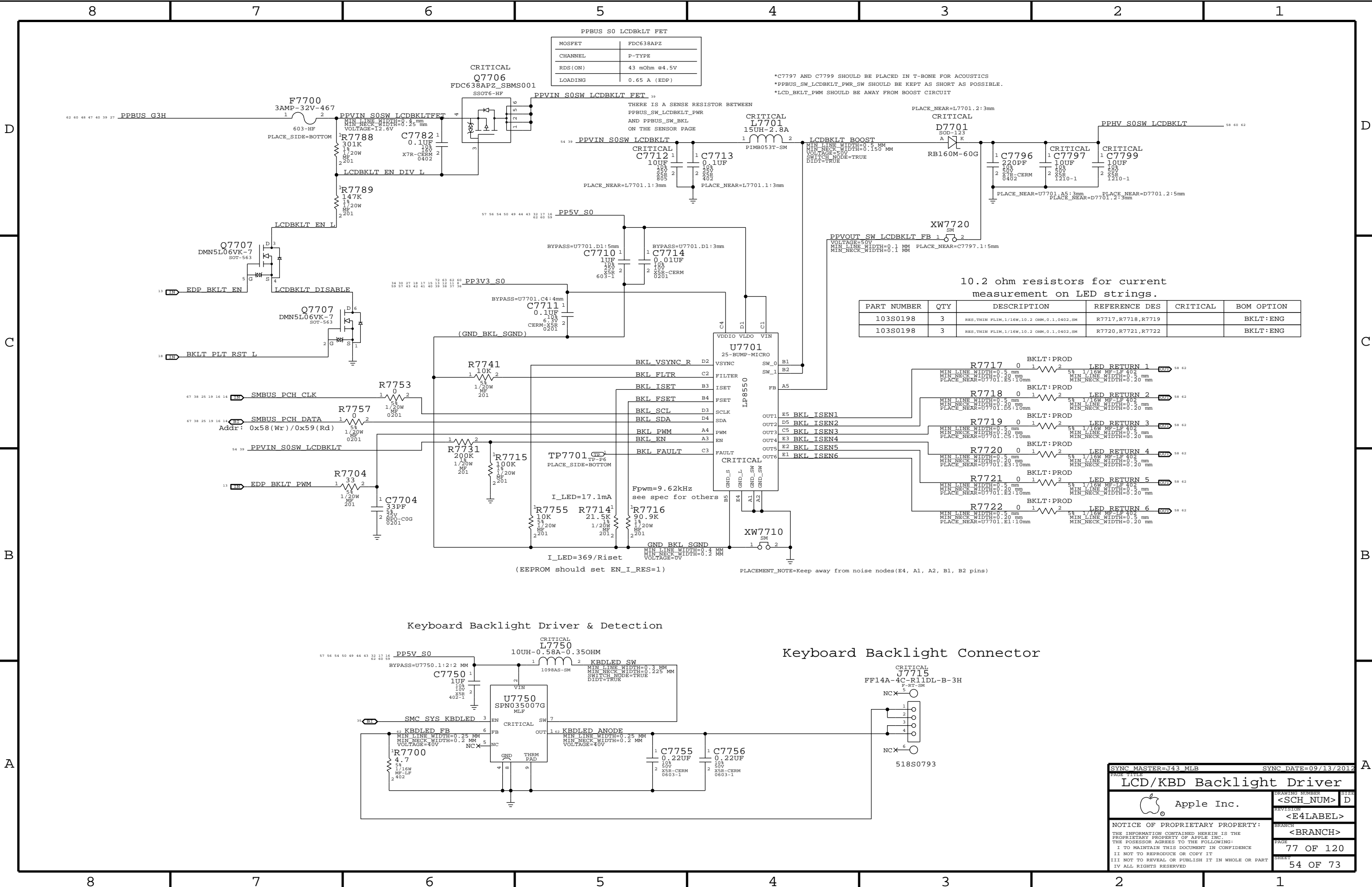
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LPDDR3 Supply			
	Apple Inc.		
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1.05V S0 Regulator



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1.05V S0 Power Supply			
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PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.


Keyboard Backlight Driver & Detection

Keyboard Backlight Connector

SYNC MASTER=J43 MLB

SYNC DATE=09/13/2012

LCD/KBD Backlight Driver

 Apple Inc.

DRAWING NUMBER

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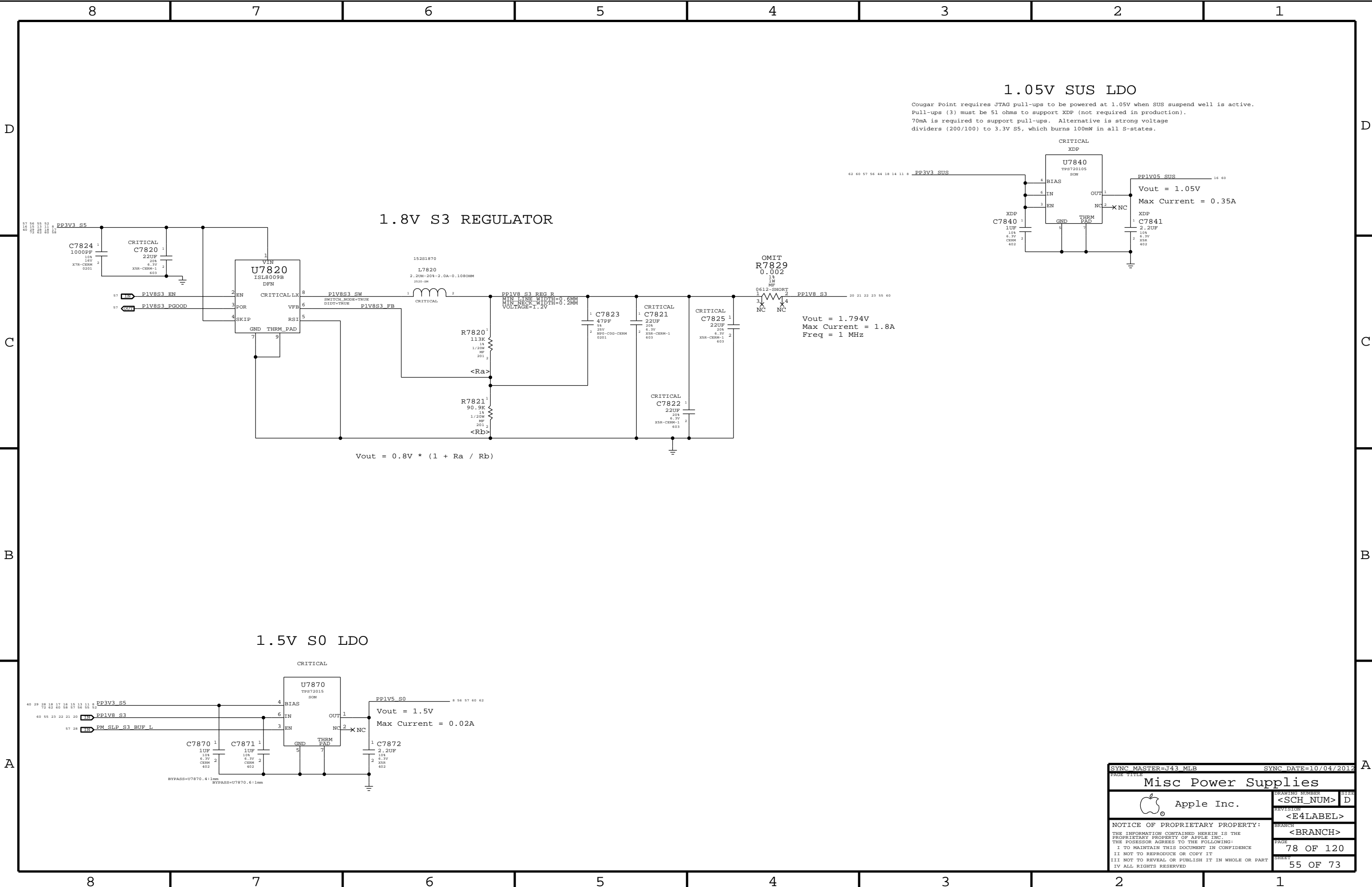
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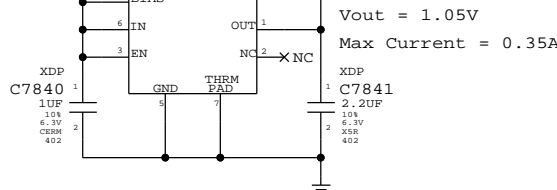
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1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

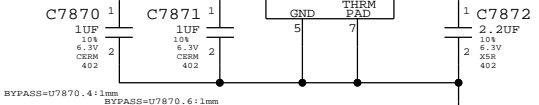



1.8V S3 REGULATOR

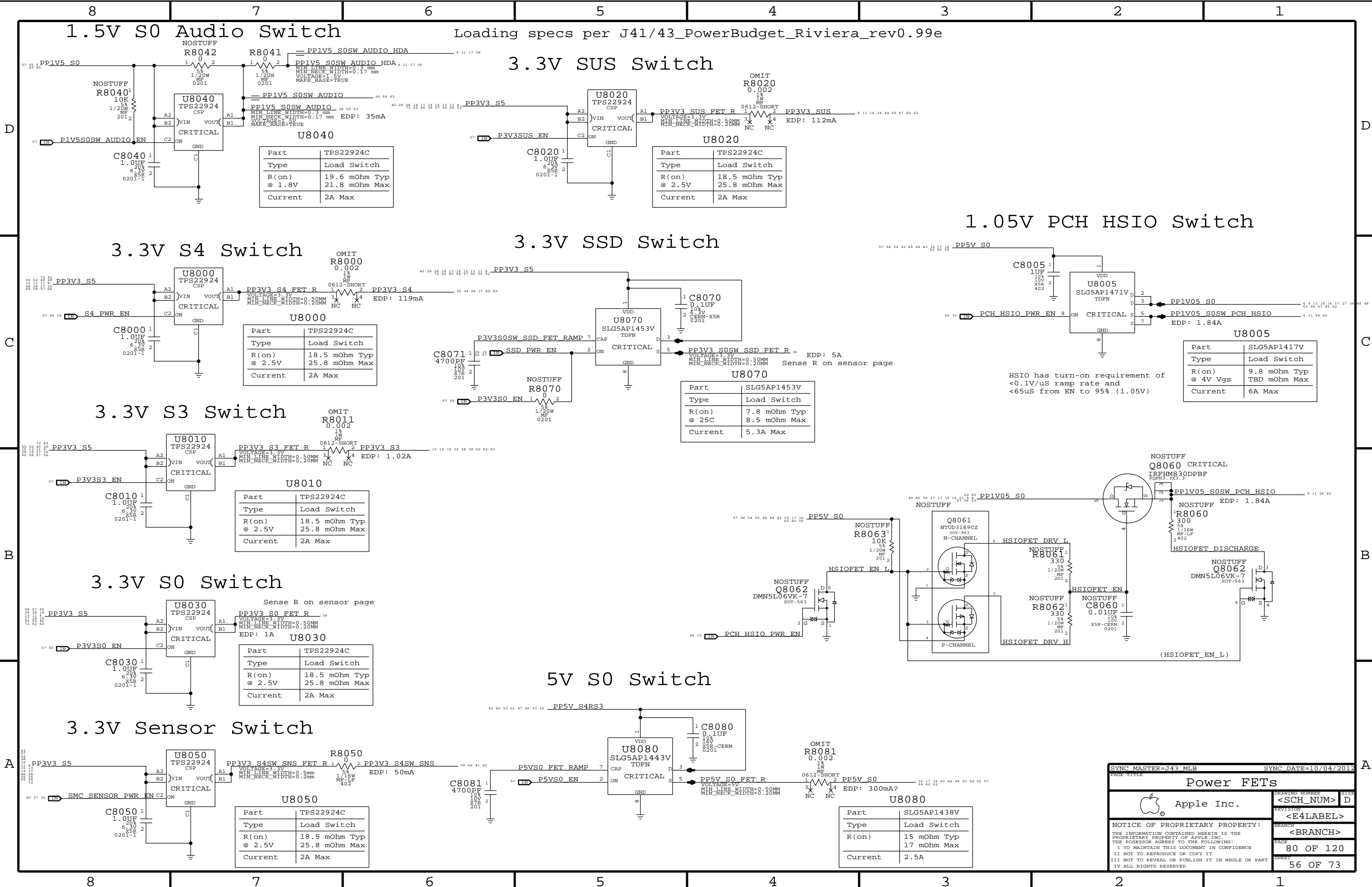
Vout = 1.794V
Max Current = 1.8A
Freq = 1 MHz

1.5V S0 LDO

Vout = 1.5V
Max Current = 0.02A



SYNC MASTER=J43 MLB		SYNC DATE=10/04/2012	
PAGE TITLE			
Misc Power Supplies			
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Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

3.3V SUS Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V SSD Switch

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

Part	SLG5AP1471V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

5V S0 Switch

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

SYNC MASTER=J43 MLB

SYNC DATE=10/04/2012

Power FETs

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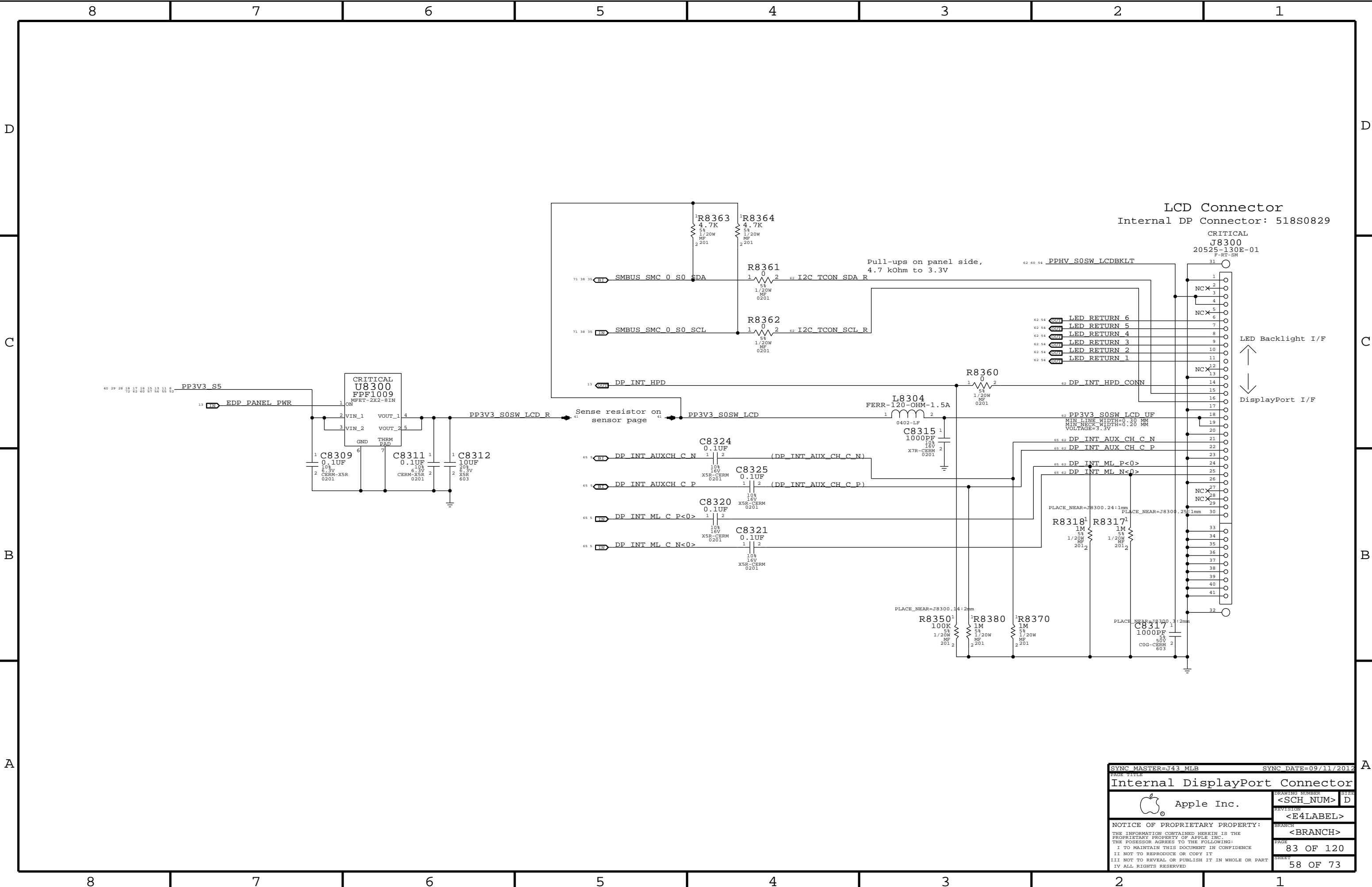
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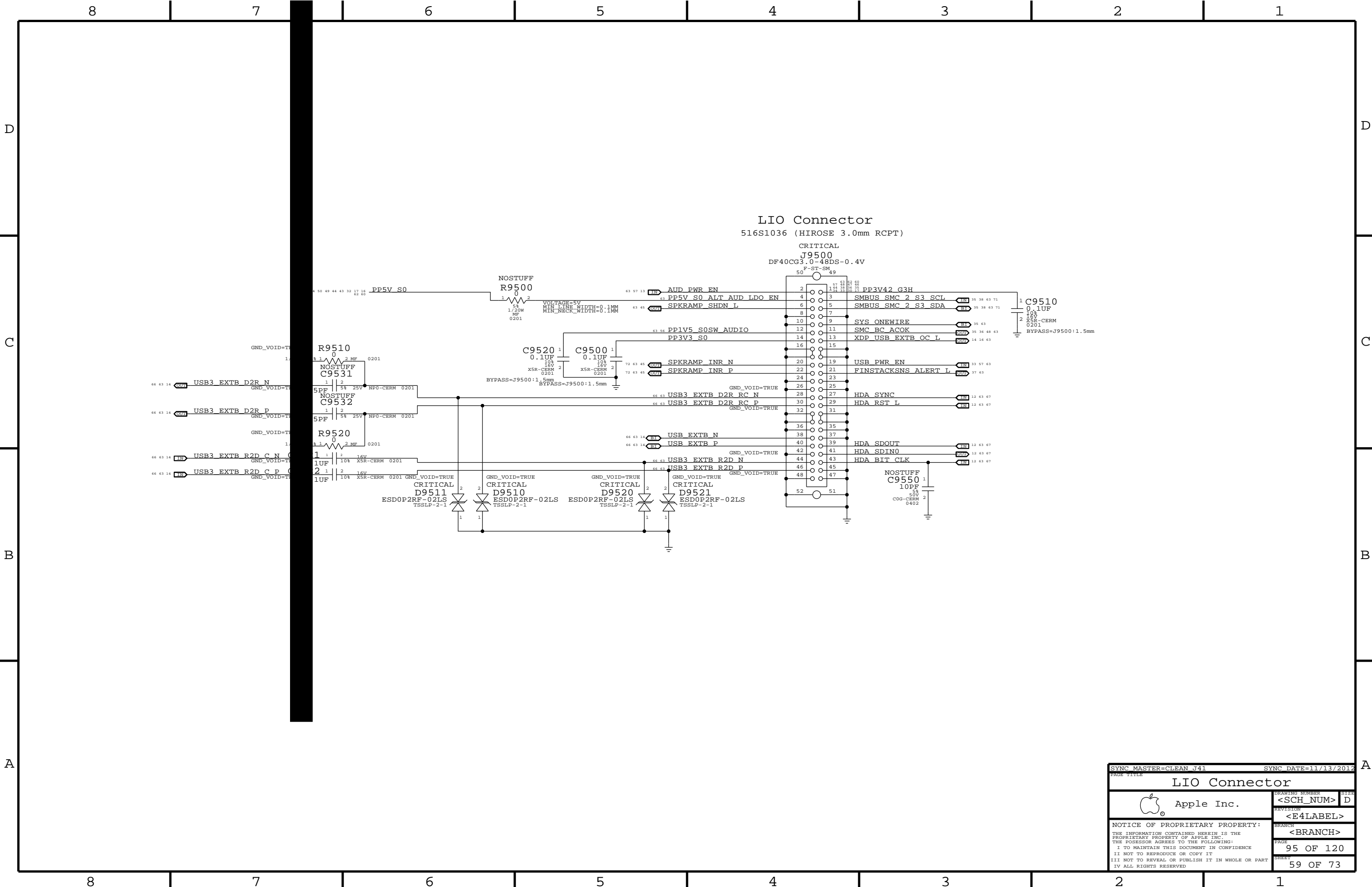
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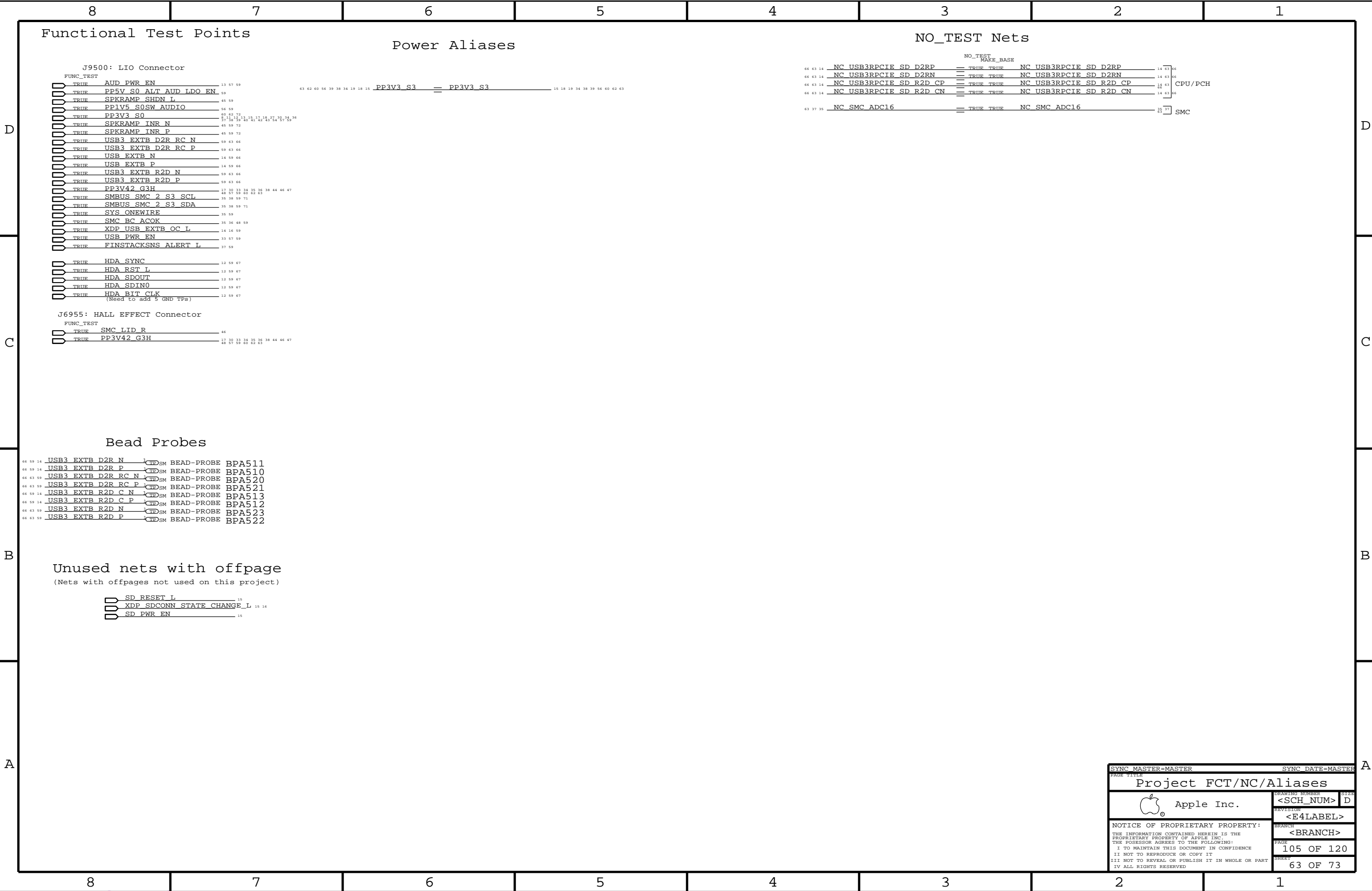
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LIO Connector			
	DRAWING NUMBER		SIZE
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8	7	6	5	4	3	2	1
Functional Test Points							
J3501: AirPort / BT Connector							
J6000: Fan Connector							
Misc Voltages & Control Signals							
J4800: IPD Flex Connector							
J7000: DC-In Connector							
J6404: Speaker Connector							
J6950: Battery Connector							
J8300: Internal DP Connector							
J6100: LPC+SPI Connector							
J7715: KB BKLt Connector							
J1800: XDP Connector							
NO_TEST Nets							
CPU/PCH							
SMC							
TBT							
Unused nets with offpage							
(Nets with offpages not used on this project)							
HDD PWR EN							
WOL EN							
BT PWRRST L							
HDMITBTMUX FLAG L							
FW PWR EN							
FW PME L							
ENET MEDIA SENSE							
LCD PSR EN							
LCD IRO L							
ODD PWR EN L							
ENET LOW PWR							
AUD IP PERIPHERAL DET							
AUD I2C INT L							
AUD IPHS SWITCH EN							
GND							
8	7	6	5	4	3	2	1



8

7

6

5

4

3

2

1

J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS			BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA, MEM_TERM		MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3, ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4, ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3, ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

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CPU Signal Constraints																																																																																																															
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<table><tr><th>NET_SPACING_TYPE1</th><th>NET_SPACING_TYPE2</th><th>AREA_TYPE</th><th>SPACING_RULE_SET</th></tr><tr><td>PCIE_CPU_TX</td><td>PCIE_CPU_TX</td><td>*</td><td>PCIE_TX2TX</td></tr><tr><td>PCIE_CPU_RX</td><td>PCIE_CPU_RX</td><td>*</td><td>PCIE_RX2RX</td></tr><tr><td>PCIE_CPU_TX</td><td>*_CPU_TX</td><td>*</td><td>PCIE_TX2OTHERTX</td></tr><tr><td>PCIE_CPU_RX</td><td>*_CPU_RX</td><td>*</td><td>PCIE_RX2OTHERRX</td></tr><tr><td>PCIE_CPU_TX</td><td>*_CPU_RX</td><td>*</td><td>PCIE_TX2RX</td></tr><tr><td>PCIE_CPU_RX</td><td>*_CPU_TX</td><td>*</td><td>PCIE_RX2TX</td></tr><tr><td>PCIE_CPU_TX</td><td>*_TX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_CPU_RX</td><td>*_TX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_CPU_TX</td><td>*_RX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_CPU_RX</td><td>*_RX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_CPU_TX</td><td>*</td><td>*</td><td>PCIE_2OTHER</td></tr><tr><td>PCIE_CPU_RX</td><td>*</td><td>*</td><td>PCIE_2OTHER</td></tr></table> <table><tr><th>NET_SPACING_TYPE1</th><th>NET_SPACING_TYPE2</th><th>AREA_TYPE</th><th>SPACING_RULE_SET</th></tr><tr><td>PCIE_PCH_TX</td><td>PCIE_PCH_TX</td><td>*</td><td>PCIE_TX2TX</td></tr><tr><td>PCIE_PCH_RX</td><td>PCIE_PCH_RX</td><td>*</td><td>PCIE_RX2RX</td></tr><tr><td>PCIE_PCH_TX</td><td>*_PCH_TX</td><td>*</td><td>PCIE_TX2OTHERTX</td></tr><tr><td>PCIE_PCH_RX</td><td>*_PCH_RX</td><td>*</td><td>PCIE_RX2OTHERRX</td></tr><tr><td>PCIE_PCH_TX</td><td>*_PCH_RX</td><td>*</td><td>PCIE_TX2RX</td></tr><tr><td>PCIE_PCH_RX</td><td>*_PCH_TX</td><td>*</td><td>PCIE_RX2TX</td></tr><tr><td>PCIE_PCH_TX</td><td>*_TX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_PCH_RX</td><td>*_TX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_PCH_TX</td><td>*_RX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_PCH_RX</td><td>*_RX</td><td>*</td><td>PCIE_2OTHERHS</td></tr><tr><td>PCIE_PCH_TX</td><td>*</td><td>*</td><td>PCIE_2OTHER</td></tr><tr><td>PCIE_PCH_RX</td><td>*</td><td>*</td><td>PCIE_2OTHER</td></tr></table>								NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX	PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX	PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX	PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX	PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX	PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX	PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS	PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS	PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS	PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS	PCIE_CPU_TX	*	*	PCIE_2OTHER	PCIE_CPU_RX	*	*	PCIE_2OTHER	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX	PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX	PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX	PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX	PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX	PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX	PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS	PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS	PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS	PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS	PCIE_PCH_TX	*	*	PCIE_2OTHER	PCIE_PCH_RX	*	*	PCIE_2OTHER
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET																																																																																																												
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX																																																																																																												
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX																																																																																																												
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX																																																																																																												
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX																																																																																																												
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX																																																																																																												
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PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS																																																																																																												
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PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX																																																																																																												
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX																																																																																																												
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX																																																																																																												
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PCIE_PCH_RX	*	*	PCIE_2OTHER																																																																																																												
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET																																																																																																												
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PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX																																																																																																												
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX																																																																																																												
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Note: DisplayPort tables are on Page 113																																																																																																															
SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.																																																																																																															

CPU Net Properties				
NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 36
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 16 62
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16 62
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
CPU_CATERR_L	CPU_45S	CPU_ITP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 36
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 36 36 49
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_RMTI	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	6 16
	CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
(FSB_CBURST_1)	CPU_45S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	6 49
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	6 49
CPU_SVIDSClk	CPU_45S	CPU_COMP	CPU_VIDSClk	6 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	6 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 26
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 26
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 26
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCie SSD

DP

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CPU Constraints			
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX	USB3_TX2TX	TOP, BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX	USB3_RX2RX	TOP, BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX	USB3_TX2OTHERTX	TOP, BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX	USB3_RX2OTHERRX	TOP, BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX	USB3_TX2RX	TOP, BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX	USB3_RX2TX	TOP, BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP, BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS	USB3_2OTHER	TOP, BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_TX	*	*	USB3_2OTHER				
USB3_PCH_RX	*	*	USB3_2OTHER				

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties


[illegible]

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_QS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_QS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_QS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_QS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_QS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_QS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_QS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_QS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_QS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_QS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_QS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_QS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_QS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_QS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_QS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_QS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_QS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER


MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER

MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A ODT<0>	7 20 21 24 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM A CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM A CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM A CAA<9..0>	7 20 24 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM A CAB<9..0>	7 21 24 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM A DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM A DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM A DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM A DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM A DQ<39..32>	7 21 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM A DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM A DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM A DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS P<6>	7 21 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS N<6>	7 21 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B ODT<0>	7 22 23 24 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM B CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM B CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM B CAA<9..0>	7 22 24 61
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM B CAB<9..0>	7 23 24 61
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM B DQ<7..0>	7 61
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM B DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM B DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM B DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM B DQ<39..32>	7 23 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM B DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM B DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM B DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS P<0>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS N<0>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS P<6>	7 23 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS N<6>	7 23 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS P<7>	7 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS N<7>	7 61
		MEM_PWR	PP1V2_S3	17 19 20 21 22 23 40
		MEM_PWR	PP0V6_S3 MEM VREFCA A	18 19 20 21
		MEM_PWR	PP0V6_S3 MEM VREFDO A	18 19 20 21
		MEM_PWR	PP0V6_S3 MEM VREFCA B	18 19 22 23
		MEM_PWR	PP0V6_S3 MEM VREFDO B	18 19 22 23

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

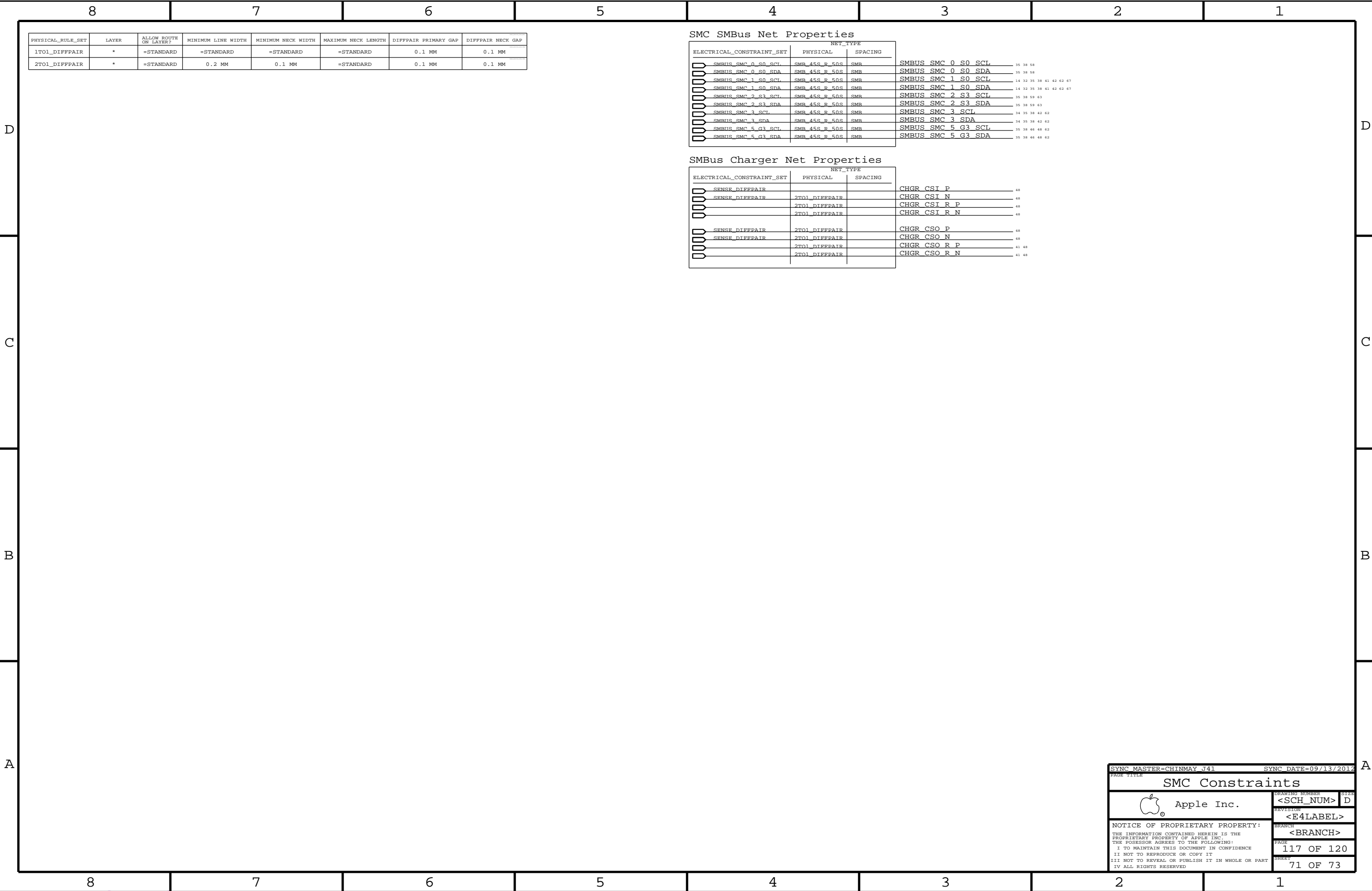
Memory to GND Spacing

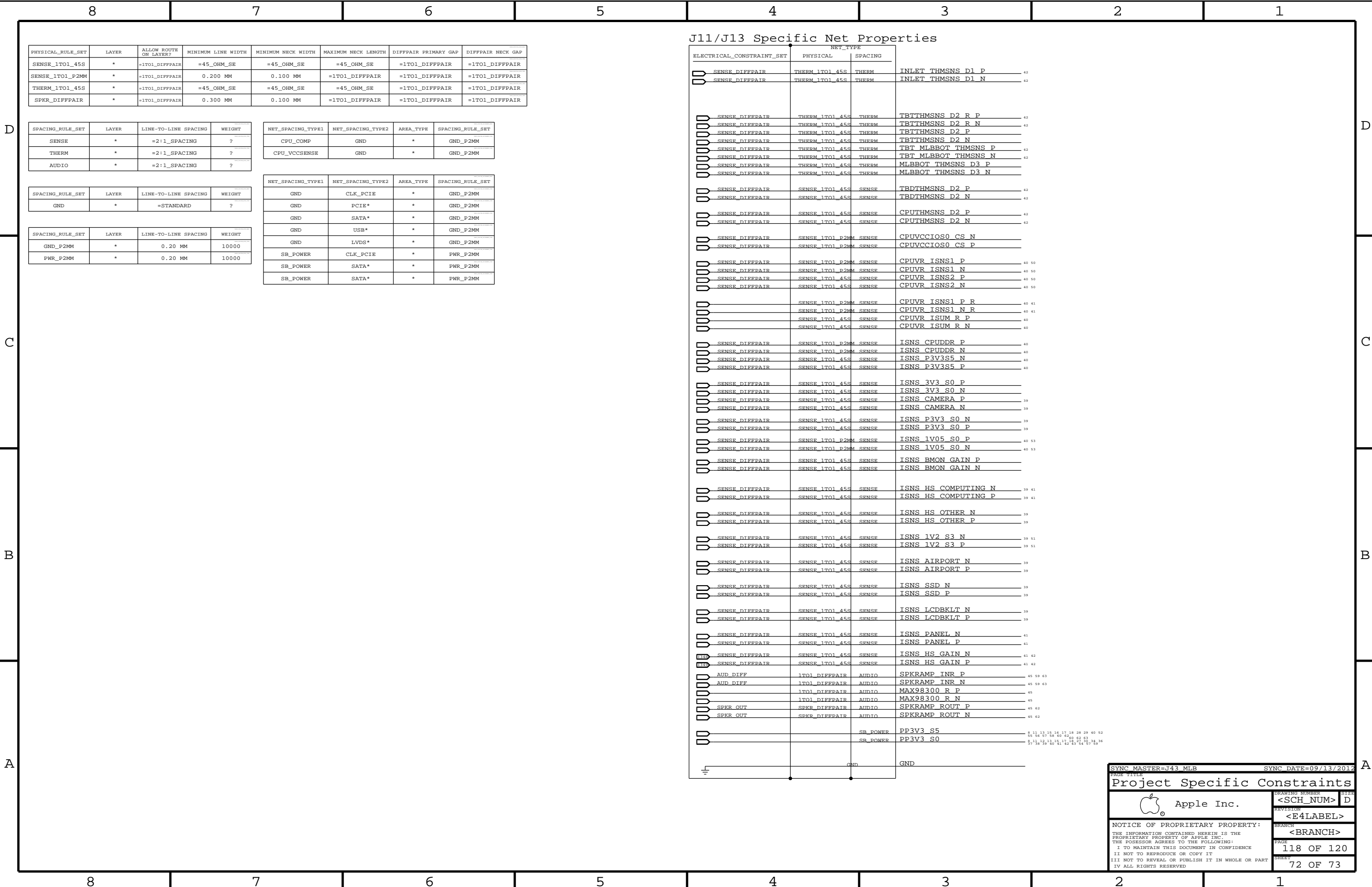
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 62
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 62
PPIV35_CAM		S2_MEM_PWR	PPIV35_CAM	31 32
PPOV675_CAM_VREF		S2_MEM_PWR	PPOV675_CAM_VREF	31 32
PPOV675_MEM_CAM_VREFCA		S2_MEM_PWR	PPOV675_MEM_CAM_VREFCA	32
PPOV675_MEM_CAM_VREFDQ		S2_MEM_PWR	PPOV675_MEM_CAM_VREFDQ	32

SYNC_MASTER=CHINMAY J41		SYNC_DATE=09/07/2012	
PAGE TITLE			
Camera Constraints			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
	<E4LABEL>		
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SENSE_1T01_P2MM	*	=1T01_DIFFPAIR	0.200 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR
THERM_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SPKR_DIFFPAIR	*	=1T01_DIFFPAIR	0.300 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 P 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 N 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R P 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R N 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 P 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 N 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS P 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS N 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	MLBBOT THMSNS D3 P 42
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	MLBBOT THMSNS D3 N 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	TBDTHMSNS D2 P 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	TBDTHMSNS D2 N 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THMSNS D2 P 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THMSNS D2 N 42
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS N 42
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS P 42
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 P 40 50
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 N 40 50
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISNS2 P 40 50
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISNS2 N 40 50
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 P R 40 41
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 N R 40 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISUM R P 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISUM R N 40
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS CPUDDR P 40
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS CPUDDR N 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3S5 N 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3S5 P 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3 S0 P 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3 S0 N 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS CAMERA P 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS CAMERA N 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3 S0 N 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3 S0 P 39
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS 1V05 S0 P 40 53
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS 1V05 S0 N 40 53
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS BMON GAIN P 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS BMON GAIN N 40
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING N 39 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING P 39 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER N 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER P 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V2 S3 N 39 51
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V2 S3 P 39 51
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT N 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT P 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD N 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD P 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT N 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT P 39
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS PANEL N 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS PANEL P 41
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS GAIN N 41 42
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS GAIN P 41 42
AUD DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR P 45 59 63
AUD DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR N 45 59 63
SENSE_DIFFPAIR	1T01_DIFFPAIR	AUDIO	MAX98300 R P 45
SENSE_DIFFPAIR	1T01_DIFFPAIR	AUDIO	MAX98300 R N 45
SPKR OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT P 45 62
SPKR OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT N 45 62
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	PP3V3 S5 8 11 13 15 16 17 18 28 29 40 52
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	PP3V3 S0 55 56 57 58 59 62 60 62 63 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000 1001 1002 1003 1004 1005 1006 1007 1008 1009 1010 1011 1012 1013 1014 1015 1016 1017 1018 1019 1020 1021 1022 1023 1024 1025 1026 1027 1028 1029 1030 1031 1032 1033 1034 1035 1036 1037 1038 1039 1040 1041 1042 1043 1044 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1061 1062 1063 1064 1065 1066 1067 1068 1069 1070 1071 1072 1073 1074 1075 1076 1077 1078 1079 1080 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110 1111 1112 1113 1114 1115 1116 1117 1118 1119 1120 1121 1122 1123 1124 1125 1126 1127 1128 1129 1130 1131 1132 1133 1134 1135 1136 1137 1138 1139 1140 1141 1142 1143 1144 1145 1146 1147 1148 1149 1150 1151 1152 1153 1154 1155 1156 1157 1158 1159 1160 1161 1162 1163 1164 1165 1166 1167 1168 1169 1170 1171 1172 1173 1174 1175 1176 1177 1178 1179 1180 1181 1182 1183 1184 1185 1186 1187 1188 1189 1190 1191 1192 1193 1194 1195 1196 1197 1198 1199 1200 1201 1202 1203 1204 1205 1206 1207 1208 1209 1210 1211 1212 1213 1214 1215 1216 1217 1218 1219 1220 1221 1222 1223 1224 1225 1226 1227 1228 1229 1230 1231 1232 1233 1234 1235 1236 1237 1238 1239 1240 1241 1242 1243 1244 1245 1246 1247 1248 1249 1250 1251 1252 1253 1254 1255 1256 1257 1258 1259 1260 1261 1262 1263 1264 1265 1266 1267 1268 1269 1270 1271 1272 1273 1274 1275 1276 1277 1278 1279 1280 1281 1282 1283 1284 1285 1286 1287 1288 1289 1290 1291 1292 1293 1294 1295 1296 1297 1298 1299 1300 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310 1311 1312 1313 1314 1315 1316 1317 1318 1319 1320 1321 1322 1323 1324 1325 1326 1327 1328 1329 1330 1331 1332 1333 1334 1335 1336 1337 1338 1339 1340 1341 1342 1343 1344 1345 1346 1347 1348 1349 1350 1351 1352 1353 1354 1355 1356 1357 1358 1359 1360 1361 1362 1363 1364 1365 1366 1367 1368 1369 1370 1371 1372 1373 1374 1375 1376 1377 1378 1379 1380 1381 1382 1383 1384 1385 1386 1387 1388 1389 1390 1391 1392 1393 1394 1395 1396 1397 1398 1399 1400 1401 1402 1403 1404 1405 1406 1407 1408 1409 1410 1411 1412 1413 1414 1415 1416 1417 1418 1419 1420 1421 1422 1423 1424 1425 1426 1427 1428 1429 1430 1431 1432 1433 1434 1435 1436 1437 1438 1439 1440 1441 1442 1443 1444 1445 1446 1447 1448 1449 1450 1451 1452 1453 1454 1455 1456 1457 1458 1459 1460 1461 1462 1463 1464 1465 1466 1467 1468 1469 1470 1471 1472 1473 1474 1475 1476 1477 1478 1479 1480 1481 1482 1483 1484 1485 1486 1487 1488 1489 1490 1491 1492 1493 1494 1495 1496 1497 1498 1499 1500 1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513 1514 1515 1516 1517 1518 1519 1520 1521 1522 1523 1524 1525 1526 1527 1528 1529 1530 1531 1532 1533 1534 1535 1536 1537 1538 1539 1540 1541 1542 1543 1544 1545 1546 1547 1548 1549 1550 1551 1552 1553 1554 1555 1556 1557 1558 1559 1560 1561 1562 1563 1564 1565 1566 1567 1568 1569 1570 1571 1572 1573 1574 1575 1576 1577 1578 1579 1580 1581 1582 1583 1584 1585 1586 1587 1588 1589 1590 1591 1592 1593 1594 1595 1596 1597 1598 1599 1600 1601 1602 1603 1604 1605 1606 1607 1608 1609 1610 1611 1612 1613 1614 1615 1616 1617 1618 1619 1620 1621 1622 1623 1624 1625 1626 1627 1628 1629 1630 1631 1632 1633 1634 1635 1636 1637 1638 1639 1640 1641 1642 1643 1644 1645 1646 1647 1648 1649 1650 1651 1652 1653 1654 1655 1656 1657 1658 1659 1660 1661 1662 1663 1664 1665 1666 1667 1668 1669 1670 1671 1672 1673 1674 1675 1676 1677 1678 1679 1680 1681 1682 1683 1684 1685 1686 1687 1688 1689 1690 1691 1692 1693 1694 1695 1696 1697 1698 1699 1700 1701 1702 1703 1704 1705 1706 1707 1708 1709 1710 1711 1712 1713 1714 1715 1716 1717 1718 1719 1720 1721 1722 1723 1724 1725 1726 1727 1728 1729 1730 1731 1732 1733 1734 1735 1736 1737 1738 1739 1740 1741 1742 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752 1753 1754 1755 1756 1757 1758 1759 1760 1761 1762 1763 1764 1765 1766 1767 1768 1769 1770 1771 1772 1773 1774 1775 1776 1777 1778 1779 1780 1781 1782 1783 1784 1785 1786 1787 1788 1789 1790 1791 1792 1793 1794 1795

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